TI PAL
303A-006 P/T ADAPTER

981-0175-005 OCTOBER 85

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NOTE

Before using this adapter, read the LogicPak™ manual.*

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Applies to: Engineering Part Numbers 715-1006-003
Text Reference Number 090-0061-005

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SECTION 1

INTRODUCTION

1.1 OVERVIEW

The 303A-006 Texas Instruments (TI) PAL® programming/testing (P/T) adapter consists of two zero-insertion force sockets with interface circuitry and EPROM (erasable, programmable read-only memory) mounted in a metal frame; see figure 1-1. The P/T adapter is used with the Data I/O 303A LogicPak™ to match programming electronics to the specific device family you are using. Any firmware unique to the TI PAL programmable logic devices is resident in the EPROM on the P/T adapter; all other necessary firmware is in the LogicPak™ or the programmer.

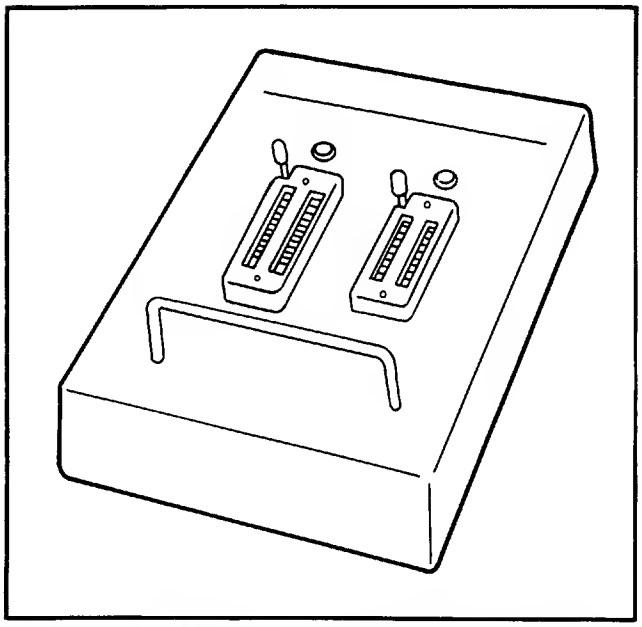

Figure 1-1. 303A-006 TI PAL Programming/Testing Adapter

This manual describes how to use the TI PAL P/T adapter. Subjects addressed in this manual and their corresponding sections are listed in table 1-1. Use this table as a quick reference point for the major sections.

In this manual, we will refer to the operational procedures for the 29A Universal Programmer; refer to your programmer manual for System 19 and 100A key sequences.

The entries that you are to make from either the programmer or terminal are indicated by the entry enclosed in a key symbol. For example,

® PAL is a registered trademark of Monolithic Memories, Inc.

Table 1-1. Using the TI PAL Programming/Testing Adapter Manual

SUBJECT	SECTION
Applications	1.2
Installation procedures for P/T adapter	2.2
Basic operation instructions	3.0
System commands	3.5
Calibration	4.2
Measurement chart for DC calibration tests	4.2
Error codes	4.2
Timing diagrams	4.2
Circuit description	5.0
Family and pinout codes	Appendix A
Functional diagrams	Appendix A
Data I/O Service Centers	Back of manual
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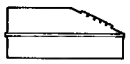
indicates that the ESCAPE key on the terminal keyboard should be pressed. In addition, the symbols shown below indicate modes of operation and prompts.

Terminal Mode



Programmer Front Panel

1.2 APPLICATIONS

Software tables resident within the P/T adapter store values for programming variables, including pinouts, voltage levels, and timing. When you choose the family and pinout codes for a particular device, the programmer uses information in these tables to assemble a specialized programming routine in scratch RAM (random-access memory). This allows high-speed operation with minimum firmware. Families with more than one pin number series (e.g., PAL 20 and PAL 24) have sockets to accommodate each pin count.

The family code and pinout code table (table A-1, appendix A) lists all the devices that can be programmed and/or tested with this P/T adapter. Table A-1 also lists the development aids as well as the family code and pin code corresponding to each device. This table will be updated as new devices are added. As Data I/O increases the capabilities of the LogicPak™ to program new devices, firmware and/or hardware updates will be available for existing adapters to add new devices to existing device families. New adapters will also be added to accommodate new device families. Contact Data I/O for the latest revision and any required firmware updates.

If a fuse pattern is generated on a host system, it must use fuse numbers specified according to the logic diagrams in this manual and transmitted to the programmer in the JEDEC (Joint Electron Device Engineering Council) format (see appendix A of the LogicPak™ manual). Data I/O uses the JEDEC Logic Device Translation Format (number JC-42, 1-81-62) for serial data input and output with the LogicPak™. The only exception to this is when you are using a Signetics H&L design adapter, in which case data transfer can also occur in the Signetics H&L logic format.

NOTE

Before operating, see the JEDEC format specifications limitations in the LogicPak™ manual, appendix A, section 3.0.

1.3 DEVICE-SPECIFIC INFORMATION (Logic Fingerprint™ Test Limitations)

The pseudorandom nature of the input vectors generated during the Logic Fingerprint™ test can cause some devices in some programming circumstances to fail by giving nonrepetitive results. THIS DOES NOT NECESSARILY INDICATE A FAULTY DEVICE, but may be an indication that the device is subject to Logic Fingerprint™ test limitations. The device may still function in the system for which it was designed. The error flag indicating the Logic Fingerprint™ test failed is alerting you that this programmed pattern may not function for all possible input states.

Table 1-2 lists the devices and their Logic Fingerprint™ test limitations. Limitation 1 occurs when devices are programmed so that nonregistered outputs are fed back to product inputs, which results in an oscillation. This condition is shown in the simplified example in figure 1-2. The two nonregistered product outputs (pins 19 and 18) in figure 1-2 feed back to the other product's input. If input pins 2 and 3 are both true (i.e., TTL "1"), the PAL will oscillate. This condition could exist for one product output feeding back to its own input or numerous outputs feeding back.

Table 1-2. Logic Fingerprint™ Test Limitations for TI PAL

Part Numbers	Logic Fingerprint™ Test Limitations
PAL16L8A	1,2
PAL16R4A	1,2,3
PAL16R6A	1,2,3
PAL16R8A	1,2,3
TIBPAL16L8	1,2
TIBPAL16R4	1,2
TIBPAL16R6	1,2
TIBPAL16R8	1,2
PAL20L8A	1,2
PAL20R4A	1,2
PAL20R6A	1,2
PAL20R8A	1,2
TIBPALR19L8	1,2
TIBPALR19R4	1,2
TIBPALR19R6	1,2
TIBPALR19R8	1,2
TIBPALT19L8	1,2
TIBPALT19R4	1,2
TIBPALT19R6	1,2
TIBPALT19R8	1,2

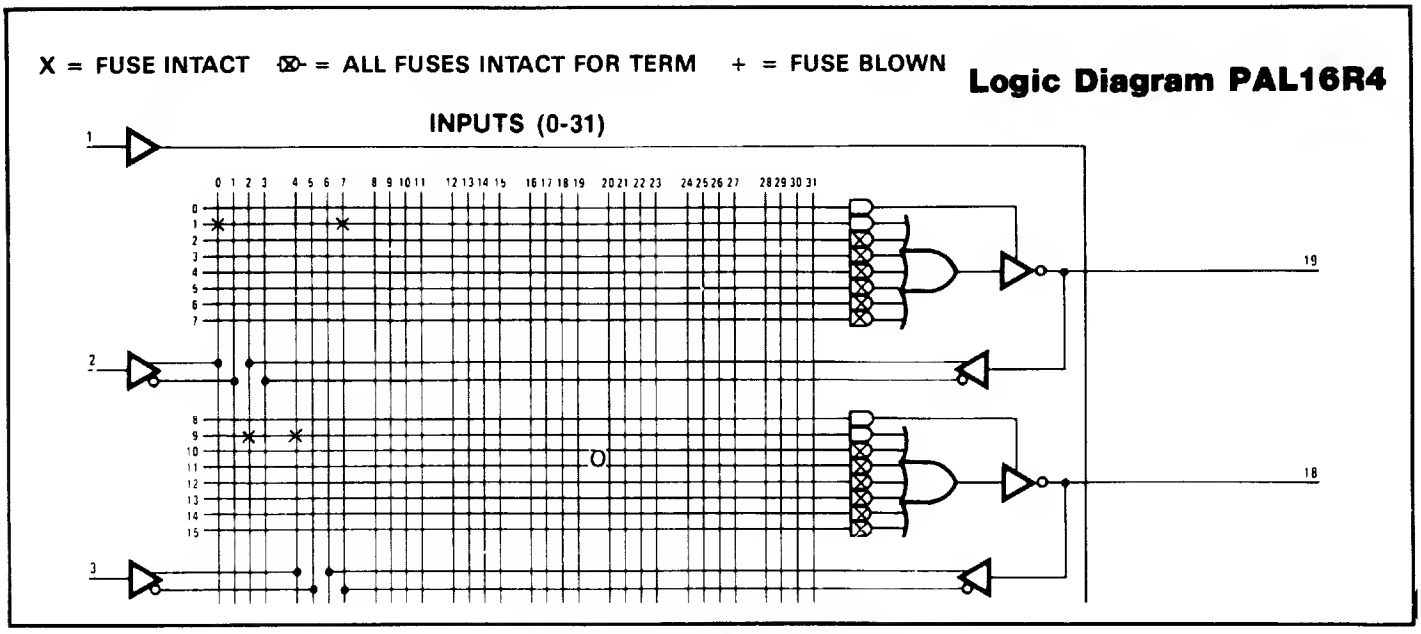


Figure 1-2. Example of Limitation 1

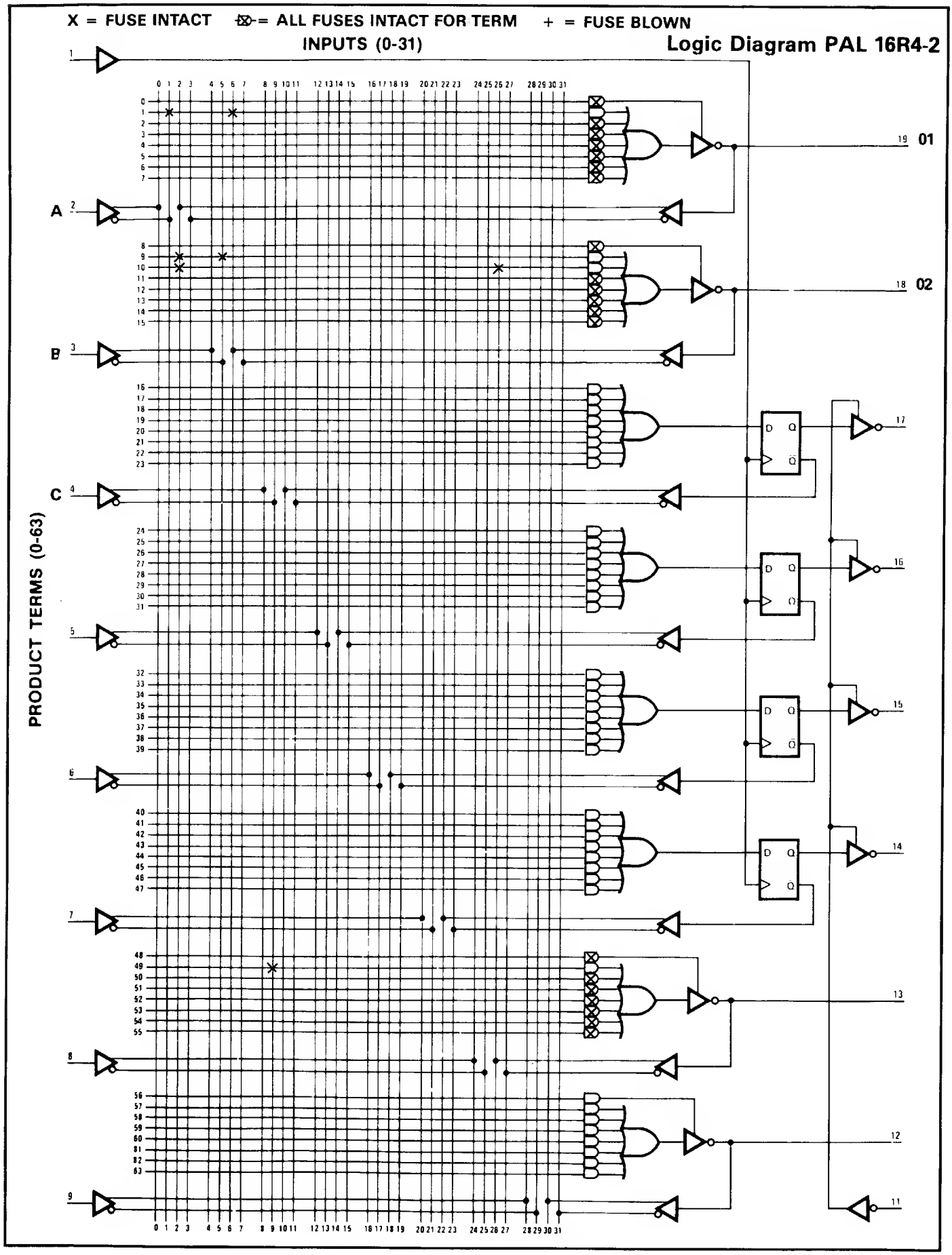
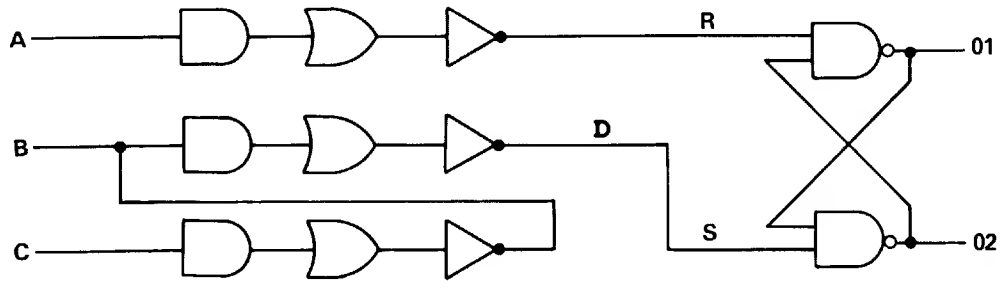


Figure 1-3. Example of Limitation 2



RS TRUTH TABLE

R	S	01	02
0	0	1	1
0	1	1	0
1	0	0	1
1	1	a	a

[a] Remains unchanged

BOOLEAN EQUATIONS

$01 = \overline{02*R}$

$02 = \overline{01*S}$

$\boxed{\overline{01} = 02*\bar{A}}$

$\overline{02} = 01*[\overline{B*C}]$

$= 01*[\bar{B} + C]$

$\boxed{\overline{02} = (01*\bar{B}) + (01*C)}$

$R = \bar{A}$

$S = \overline{B*C}$

Figure 1-4. Example of Limitation 2 With Truth Table and Boolean Equations

Limitation 2 occurs when a race condition is programmed into the device. Because the inputs are controlled, it is possible that the race condition will not be critical in the circuit for which the device was designed. Due to the random nature of the inputs during the Logic Fingerprint™ test, the race condition could appear and cause unstable results. An RS latch is an example of this. Figures 1-3 and 1-4 show the schematic, truth table, Boolean equations, and fuse map. Suppose that A, B, and C are at logic lows, 01 is at a logic high, and 02 is at a logic low. Let B and C go to a logic high simultaneously. The state of D will depend on how fast B and C can propagate through the logic gates. The effect of B will arrive at D first, forcing it low. At a time equal to the propagation delay of the gates later, the effect of C will be seen at D, forcing it back to a logic high. When D was at a logic low, the RS latch changes state and is unaffected when D comes back high. This causes the Logic Fingerprint™ test to read the wrong values on the outputs, which in turn causes an unstable result.

If the default starting vector of Ø results in a test-sum of FFFF FFFF, select a starting vector other than Ø.

Limitation 3 occurs in registered parts only. When using the Logic Fingerprint™ test, it is mandatory to start from the same state every time the test is performed. Some registered PALs, however, will not power up into the same state every time. If the Logic Fingerprint™ test starts at a different point, it will produce unstable results. To overcome this limitation, the registered outputs must be put into a known state before executing the Logic Fingerprint™ test. Two methods are:

1. Dedicate one input line as a preset or reset line for all registered output. A starting vector can then be written to set or clear all registered outputs.

2. If no extra inputs are available to dedicate to a preset/reset line or a known state of other than all ones or all zeros is required, the setup must consist of one or more vectors to force the output into the desired state. If more than one is needed, the structured test must be used to input the vectors rather than the starting seed for the Logic Fingerprint™ test. (See the LogicPak™ manual, section 1.4.3, or, in this manual, sections 3.5.7 and 3.5.8.)

NOTE

It is important that you recognize when devices are programmed with these limitations and realize that the Logic Fingerprint™ test will reject them. These devices can still be tested by using structured test vectors.

1.4 SPECIFICATIONS

The P/T adapter receives its power from the LogicPak™ and the programmer power supplies. Programming waveforms are generated from programmer supplies using the digital-to-analog converters (DAC) controlled by the programmer's microprocessor. The controlling firmware is located both on a circuit board in the LogicPak™ and in the P/T adapters. The physical and environmental specifications of the P/T adapter are:

- altitude (operating): sea level to 3 km (10,000 ft)
- humidity (operating): 90% maximum (noncondensing)
- humidity (storage): 95% maximum (noncondensing)
- temperature (operating): −5 to 45°C (41 to 113°F)
- temperature (storage): −40 to 70°C (−40 to 158°F)
- weight: .255 kg (9 oz)
- dimensions: 16.6 x 12.3 x 2.1 cm (6.54 x 4.84 x .81 in.)

1.5 FIELD APPLICATIONS SUPPORT

Data I/O has field applications engineers throughout the world. They can provide additional information about interfacing Data I/O products with other systems and answer questions about your equipment.

These engineers are located within the United States at the addresses listed in the back of this manual. For international applications support, contact your nearest Data I/O representative.

1.6 WARRANTY

The 303A-006 P/T adapter is warranted against defects in materials and workmanship. The warranty period of 90 days begins when you receive the equipment; the warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

1.7 SERVICE

Data I/O maintains service centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. A list of all service centers is located in the back of this manual.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative. Orders for shipment must include:

- a description of the equipment (see the latest Data I/O price list or contact your sales representative for equipment and part numbers)
- purchase order number
- desired method of shipment
- quantity of each item ordered
- shipping and billing address of the firm, including ZIP code
- name of person ordering the equipment

SECTION 2

INSTALLATION

2.1 INSPECTION

The P/T adapter was thoroughly tested and inspected before shipment and was carefully packaged to prevent shipping damage. Inspect your adapter to ensure that no damage occurred during shipment. If you notice any damage, file a claim with the carrier and notify Data I/O.

2.2 ADAPTER INSTALLATION

To insert the P/T adapter into the LogicPak™:

1. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.4.3.
2. Align the guide pins on the underside of the adapter with the guide pin holes on the LogicPak™ (see figure 2-1).
3. Gently set the adapter on the LogicPak™.
4. Firmly press down on the front edge of the adapter to lock the connector pins into the connector receptacle (see figure 2-1).

2.3 ADAPTER REMOVAL

CAUTION

BEFORE REMOVING THE ADAPTER, press ESC from the terminal, or, from the programmer front panel, press the KEYBOARD key (on the System 19) or the VERIFY key (on the 100A or 29A). Because the processor in the programmer executes firmware resident in the adapter, these precautions must be taken before removing the adapter from the LogicPak™ to prevent a program interrupt or loss of RAM data.

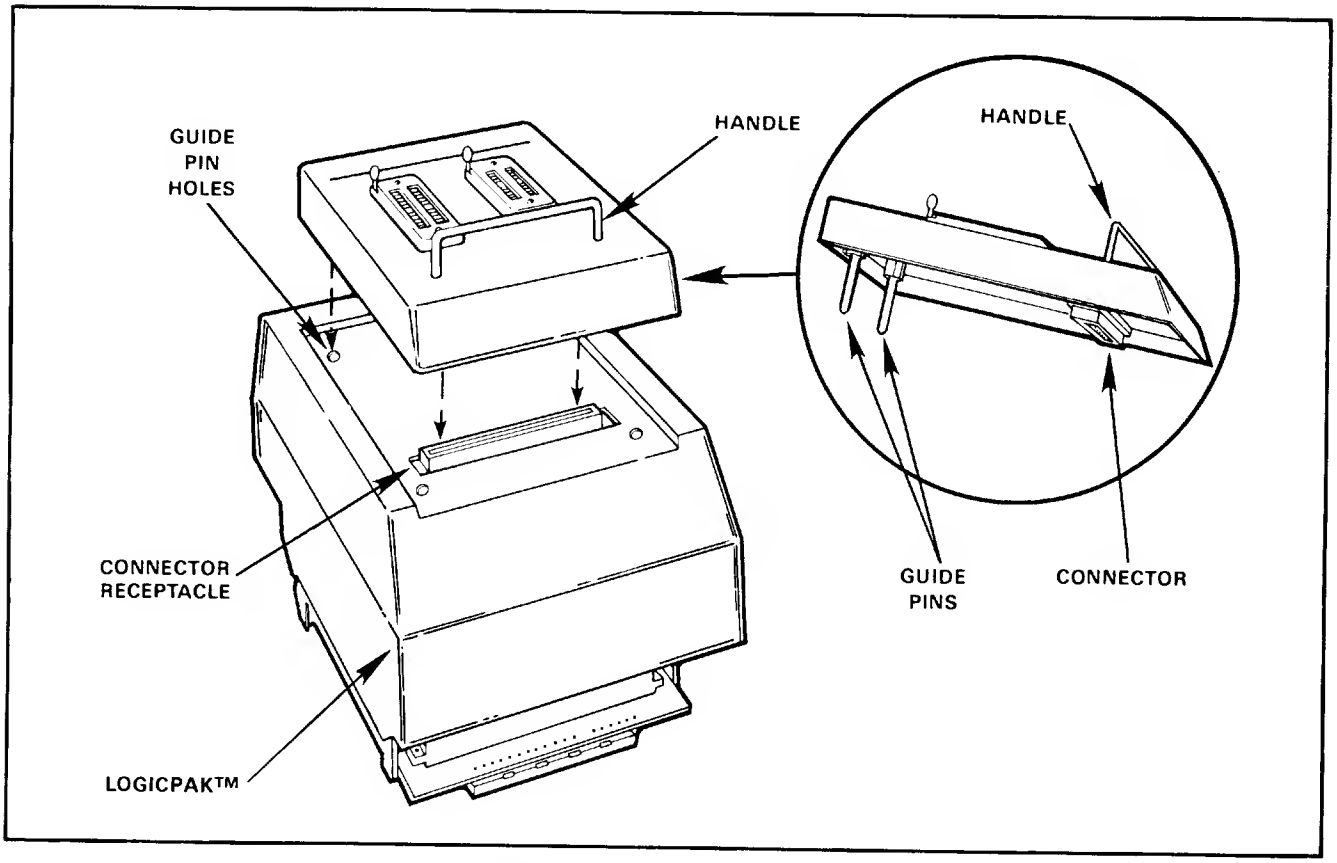


Figure 2-1. Adapter Installation

To remove the adapter:

1. Ensure that the programmer has completed the current operation.
2. Ensure that a device is not in a socket.
3. While holding down the LogicPak™, grasp the adapter handle and gently remove the adapter.

2.4 REPACKING FOR SHIPMENT

If the adapter is to be shipped to Data I/O for service or repair, attach a tag to it describing the work required and identifying the owner. In correspondence, identify the unit by part number, revision level, and the name of the unit. If the original shipping container is to be used, place the adapter in the container with the appropriate packing materials, and seal the container with strong tape. If another container is used, be sure that it is a heavy carton, wrapped with heavy paper or plastic; use appropriate packing material, and seal well with strong tape. Mark the container "DELICATE INSTRUMENT" or "FRAGILE."

SECTION 3

OPERATION

3.1 OVERVIEW

The 303A-006 P/T adapter enables you to program and functionally test the devices listed in table A-1 of appendix A. These logic devices are arrays of gates and flip-flops joined by matrices of fusible links. The devices can be programmed by blowing selected fuses in the matrices, which leaves the remaining intact connections to perform the desired logic functions.

The fuse pattern necessary to program a device should have already been developed using a Data I/O LogicPak™ and a design adapter or a host computer system; if you have not developed your fuse pattern, consult the LogicPak™ manual and design adapter manual to develop your data before proceeding. However, if you have entered your data in Boolean equations or function tables (truth tables), they must be translated into a fuse pattern before you can begin programming. (Don't turn the power off; if you do, you will lose all your data.) If you have not used a design adapter, the fuse pattern must be loaded from: 1) a master device, 2) the serial port, or 3) manually from a programmer or terminal keyboard.

An alternate method of specifying the fuse pattern is to manually enter the fuse number and state for every fuse in the device. Each P/T adapter manual contains logic diagrams for the devices in its repertoire. These are the same as those in the device manufacturers' data books, but the fuse numbers have been added. Although tedious, fuse numbers and states can be entered manually into the programmer's data RAM from the programmer's keyboard or from a terminal. This method usually will be used only for editing fuse data because it is a long process with room for error.

With a P/T adapter, fuse data can be entered into the programmer's RAM by loading from a master device shown in figure 3-1. Blank devices can then be programmed using the same P/T adapter, or other manufacturers' functionally equivalent second-source devices can be programmed by installing the appropriate P/T adapter. Remember that a device with its security fuse programmed cannot be used as a master because its fuses cannot be read.

```
DATA I/O CORPORATION  PLDS-PROGRAMMING/TESTING ADAPTER

0 - DISPLAY MENU                                  COPYRIGHT 1982
1 - ENTER FAMILY PIN CODE
2 - LOAD DEVICE
3 - VERIFY DEVICE
4 - PROGRAM DEVICE
5 - ENTER REJECT COUNT OPTION
6 - ENTER VERIFY OPTION
7 - ENTER LAST FUSE OPTION
8 - ENTER FUNCTIONAL TEST DATA
A - DISPLAY FUSE PATTERN
B - RECEIVE FUSE DATA
C - TRANSMIT FUSE DATA
D - DISPLAY FUSE SUMCHECK
E - ENTER DECIMAL FUSE DATA

<ESC> - BEFORE REMOVING ADAPTER

COMMAND =
```

Figure 3-1. Function Menu

Programming is controlled either from the programmer keyboard or from a terminal. Firmware in the P/T adapter automatically tests the device's position in the socket, ensures that the device is blank, and looks for illegal bits; figure 3-2 defines the overall fuse programming sequence. Programming begins when these automatic checks are completed and determined acceptable.

After the device has been programmed, it is automatically verified and tested according to options you select.

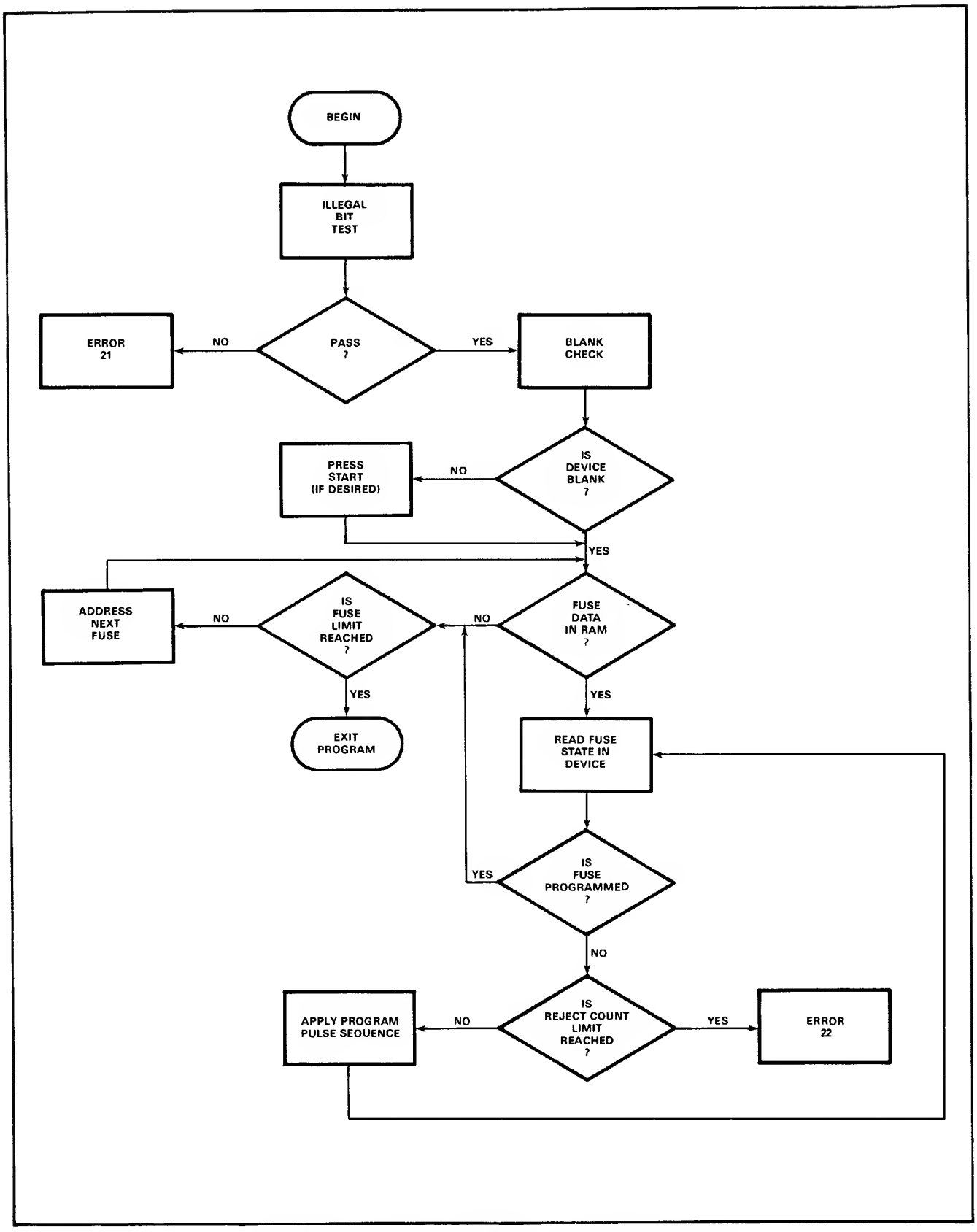


Figure 3-2. Automatic Programming Sequence Flowchart

In addition to enabling you to program and test devices, the P/T adapter also enables you to view data, change them, and/or enter test parameters. These optional steps are listed in Table 3-1. The functions of the P/T adapter are described in table 3-1 and section 3-5. Sections 1 and 3 of the LogicPak™ manual also describe these functions. Logic diagrams with decimal fuse numbers are in appendix A.

3.2 POWER UP

NOTE

If the LogicPak™ with adapter is not installed in the programmer before power is turned on, you will hear a beep until the LogicPak™ is installed.

When power is applied, the programmer will perform an automatic self-test routine. When the self-test routine is complete, the programmer will signal its readiness; see your programmer manual.

Table 3-1. PLDS System Command Summary

MODULE OR ADAPTER	COMMAND TYPE	FROM FRONT PANEL	VIA TERMINAL	COMMAND DESCRIPTION	SEE SECTION
LogicPak™ (with any adapter)		--	Ø	Display menu	3.5.2
		E 1	-	Enable terminal mode	3.5.1
		--	1	Enter family and pinout codes	3.5.3
		E 5	5[a]	Set reject count	3.5.4
		E 6	6	Select verify option	3.5.5
		E 7	7	Select security fuse option	3.5.6
		E 8	8	Set number of Logic Fingerprint™ test cycles	3.5.7
		E 9	8	Enter starting vector and test-sum	3.5.8
		--	8	Enter structured test vectors	3.5.9
		E A	A	Display fuse pattern	3.5.10
		E B	B	Receive fuse data	3.5.11
		E C	C	Transmit fuse data	3.5.12
		E D	D	Display sum-check of fuse data	3.5.13
		E E	E	Enter fuse data by fuse number	3.5.14
		E F	-	Display configuration number	3.5.15
		--	ESC	Before removing adapter	3.5.16
[a]Except with PALASM adapter.					
PALASM Design Adapter	Development	--	Ø	Display menu	Refer to PALASM Design Adapter Manual
		--	1	Enter family and pinout codes	
		E 2	2	Receive source equations	
		E 3	3	Transmit source equations	
		E 4	4	Translate source equations	
		E Ø	5	Simulate source equations	
		E 5	--	Set reject count	
	Edit	--	9	Edit mode (all commands listed below)	
		--		B Display line 1	
		--		C Replace text	
		--		D Delete text	
		--		E Display to end	
		--		I Insert/enter text	
		--		K Delete current line	
		--		L Display 24 lines	
		--		M Display commands	
		--		U Display previous line	
		--		(space bar) Move cursor/prompt right	
		--		(RUB/DEL) Move cursor/prompt left and delete during insert mode	
		--		CTRL H/ (back space) Move cursor/prompt left	
		--		CTRL M/ (carriage return) Display next line	
		--		CTRL P Purge all text	
		--		CTRL Z Exit editor/exit "C" or "I" modes of editor	
		--		ESC Before removing adapter	

NOTE: ESC (escape) returns control to programmer front panel.

Table 3-1. (Con't.)

MODULE OR ADAPTER	COMMAND TYPE	FROM FRONT PANEL	VIA TERMINAL	COMMAND DESCRIPTION	SEE SECTION
H&L Design Adapter	Development	--	Ø	Display menu	Refer to H&L Design Adapter Manual
		--	1	Enter family and pinout codes	
		E 2	2	Receive data (IFL format)[b]	
		E 3	3	Transmit data (IFL format)	
	Edit	--	4	Edit mode	
		--		G Enter gate number	
		--		P Enter product term number	
		--		T Enter transition term number	
		--		V Move cursor forward	
		--		V Move cursor backward	
		--		F Display next term	
		--		R Display last term	
		--		N Enter next field	
		--		I Insert term	
		--		D Delete term	
		--		C Clear term	
		--		X Deactivate term	
		--		E Display edit sub-menu	
		--		(Ø) Exit edit mode	
		--		(1) Return to edit mode	
		--		(2) Serial input (receive IFL format)[b]	
		--		(3) Serial output (transmit IFL format)	
		--		(4) List low-order terms	
		--		(5) List high-order terms	
		--		(6) Compress terms	
		--		CTRL Z Exit edit mode	
		--		ESC Before removing adapter	
[b]Integrated fuse logic, Signetics ASCII					
All P/T Adapters	Device	--	1	Enter family and pinout codes	3.4.1
		Load	2	Load fuse data from device to RAM	3.4.3
		Verify	3	Verify fuse data and perform functional test	3.4.5
		Program	4	Program device with RAM data	3.4.4

NOTE: ESC (escape) returns control to programmer front panel.

To turn the programmer on:

1. Check to make sure a device is not in a socket. If a device is in a socket, lift up the lever (on the upper left of the socket; see section 3.4.2), then gently lift the device out of the socket.
2. Plug the AC power cord into the power outlet.
3. Flip the power switch up to the ON position; see figure 3-3.

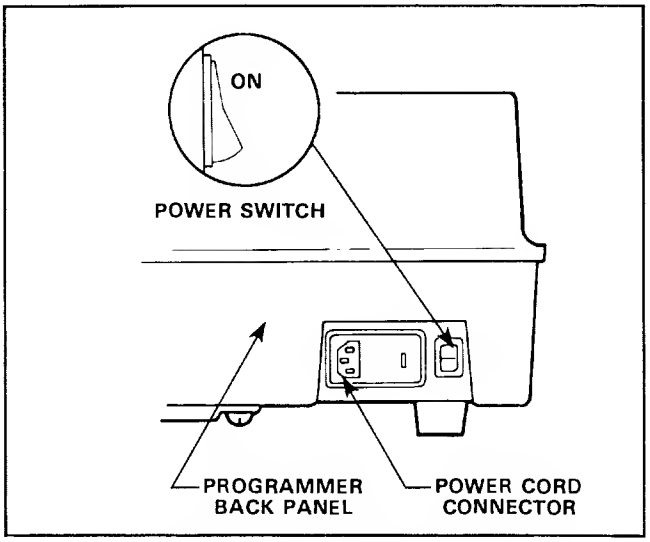


Figure 3-3. Programmer Power Switch Location

3.3 POWER DOWN

CAUTION

Do not turn the power off while the programmer is doing an operation or when a device is in a socket; voltage transients may damage the device.

To turn the programmer power off:

1. Check to make sure the programmer is not in an operation process. If it is, wait until the operation is complete.
2. Check to make sure a device is not in a socket. If a device is in a socket, remove it as described in section 3.4.3.
3. Flip the power switch down to the OFF position (figure 3-3).

3.4 BASIC DATA TRANSFER OPERATIONS

The basic operations that can be accomplished with the LogicPak™ and 29A Universal Programmer are:

- develop data
- load RAM with master device data (described in section 3.4.4)
- program a device with RAM data (described in section 3.4.5)
- verify RAM data against the device data (described in section 3.4.6)
- functionally test device (described in sections 3.5.7 through 3.5.9)

The following sections describe device-related operations with the PLDS using a P/T adapter. Most setup procedures specify that you enter the family and pinout codes. Data I/O recommends that you develop the habit of entering these codes when prompted by the equipment. However, if you are using a design adapter, you will be able to perform nondevice-related operations without entering the family and pinout codes.

If the programmer has been used to program PROMs, or for some other reason contains data in RAM, this could adversely affect the fuse pattern developed for logic devices or could inadvertently set option parameters. Therefore, execute the "clear RAM" select function (see programmer manual), or switch off the programmer to clear RAM before beginning operations with the PLDS.

All data transfer or verification operations occur between the programmer's internal RAM and the device or between the RAM and serial port in your programmer. Because the operation procedure to transfer data via a serial port varies among programmers, this manual describes only data transfer using the 29A. For other programmers, refer to the specific operation manual.

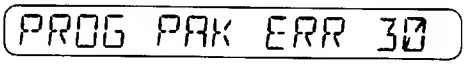
NOTE

An adapter must be installed in the LogicPak™ before any of these operations can be performed (see section 2.2).

During copy and verify operations, ADDR and SIZE appear in the 29A prompts. These correspond to starting address and block size, respectively. These block limits must remain in the default state for logic device programming. An error code (see section 4, table 4-2) will be displayed if these limits are altered. For more detail on these parameters, see your programmer manual.

3.4.1 FAMILY CODE AND PINOUT CODE SELECTION

Any device that can be programmed with the LogicPak™ is specified by a unique combination of a two-digit family code and a two-digit pinout code; these codes are provided in each adapter manual. Once the codes are entered for a particular device, the LogicPak™ remains set up for any operation with that device until you enter new codes. If invalid family and pinout codes are entered, a beep will sound. In remote control operation,



will be displayed, and the operation will be stopped when a device operation is attempted.

To select the family and pinout codes:

1. Locate the manufacturer and part number stamped on the device.
2. Go to the family and pinout code table, table A-1 in appendix A, and find the manufacturer's name.
3. Go to the column entitled "Device Part Number" and find the number corresponding to the number on the device.
4. Go to the column labeled "Family Code" and "Pinout Code" to find the code numbers corresponding to the device number for the manufacturer of the device.
5. Enter the family code and pinout code you selected from this table when prompted by the programmer or terminal. An LED (light emitting diode) will light above one of the sockets on the adapter.

3.4.2 DEVICE INSERTION

Once you have entered the appropriate family and pinout codes, the LogicPak™ is ready to accept a device in the socket below the lighted LED.

A good electrical connection between the device and the socket is essential. To ensure a good connection:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the upper-left side of the socket below the lighted LED; see figure 3-4. The lever will stay in the upright position.
3. Gently set the device in the socket below the lighted LED. Make sure pin 1 of the device is aligned with pin 1 of the socket (upper-left corner); see figure 3-4.
4. Push the lever down to lock the device in the socket.

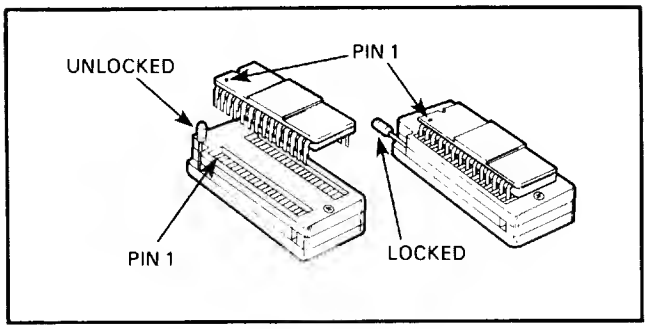


Figure 3-4. Device Installation

3.4.3 DEVICE REMOVAL

To remove a device:

1. Check to make sure the programmer is not doing an operation. If it is, wait until the operation is complete.
2. Lift the lever on the left side of the socket: see figure 3-4. The lever will remain in the upright position.
3. Lift the device out of the socket; the LED will remain illuminated.

3.4.4 LOAD RAM WITH MASTER DEVICE DATA

To load the 29A RAM with data from a master device with control from programmer front panel, follow the steps given below.

NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

1. 

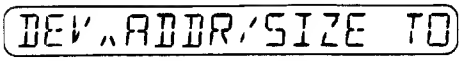
to select the mode.

29A Displays

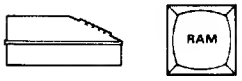
2. 

to select the source of the data.

29A Displays

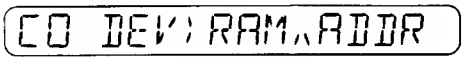


ADDR/SIZE pertains to block limit parameters. These are PROM-related and are not to be used with logic devices. Leave defaults in effect.

3. 

to select the destination for the data.

29A Displays



4. 

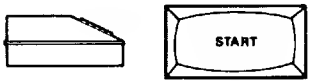
29A Displays

5. Enter the family code and pinout code (see section 3.4.1).

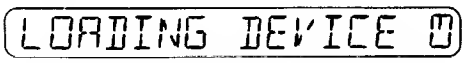
NOTE

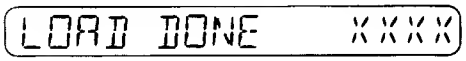
The appropriate socket LED will light.

6. Insert the master device into the appropriate P/T adapter socket. (See section 3.4.2.)

7. 

29A Displays





NOTE

XXXX is the sum-check of the device fuses.

8. Remove the master device from the LogicPak™ (see section 3.4.3).

To load the 29A with data from a master device from the terminal control mode, follow the steps given below.

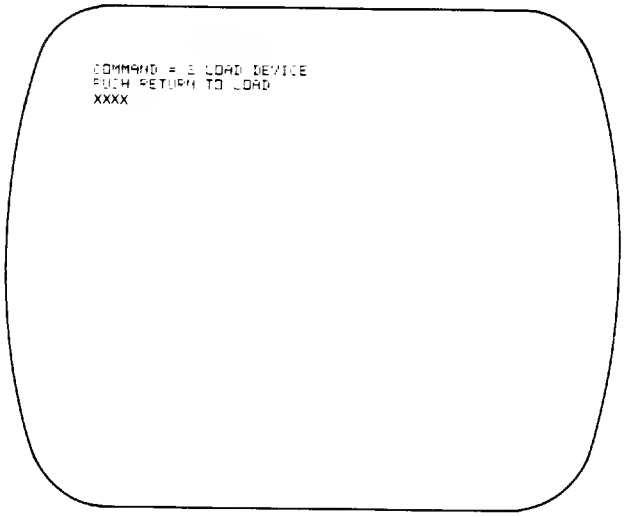
1. Place the system in terminal mode; see section 3.5.1.
2. Enter the family pinout code, if prompted by the terminal.

NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

3. 

Terminal Displays



4. 

There will be a short delay while the load operation is occurring. After the load operation is complete, the terminal will display XXXX.

NOTE

XXXX is the sum-check of the device fuses.

3.4.5 PROGRAM DEVICE WITH RAM DATA

NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

When programming a device, the system performs illegal bit tests and blank checks at nominal V_{CC}.

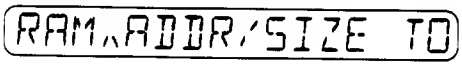
To program a blank device with the data in the 29A RAM with control from the programmer front panel, follow the steps given below.

1. 

29A Displays

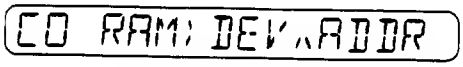
2. 

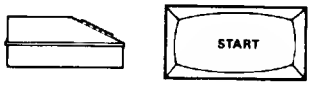
29A Displays



3. 

29A Displays

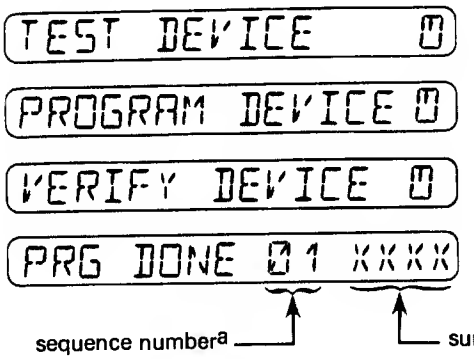


4. 

29A Displays

5. Enter the family code and pinout code (see section 3.4.1) if necessary.
6. Insert the blank device into the adapter socket (section 3.4.2).
7. 

29A Displays



[a]Increments by 1 for each device programmed.

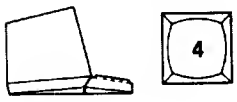
8. Remove the device from the adapter socket (see section 3.4.3).

To program a device with 29A RAM data from the terminal control mode:

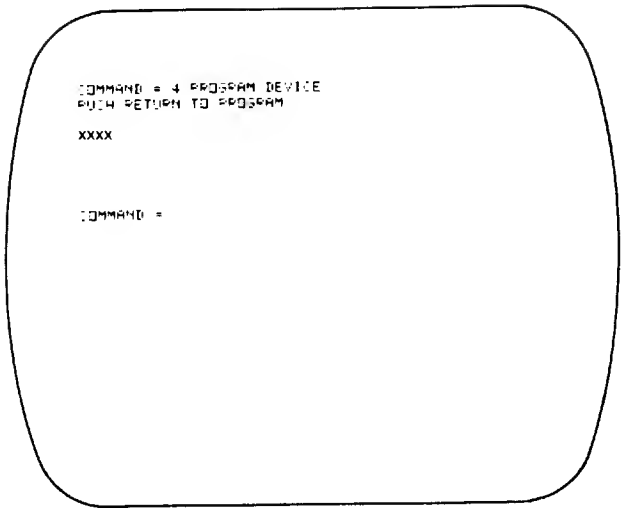
1. Place the system in the terminal mode; see section 3.5.1.
2. Enter the family pinout code, if prompted by the terminal.

NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

3. 

Terminal Displays



4. 

There will be a short delay after pressing RETURN. This is when the programmer is pretesting, programming, verifying, and functionally testing the device. If no errors occur, the terminal displays XXXX.

NOTE

XXXX is the sum-check of the device fuses.

3.4.6 VERIFY AND FUNCTIONALLY TEST DEVICE

To verify and functionally test a device from 29A front panel control follow the steps given below:

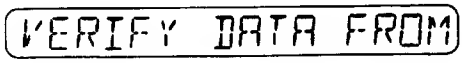
NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

The verify routine compares the device data to RAM data and performs functional testing if this option is selected.

1. 

29A Displays



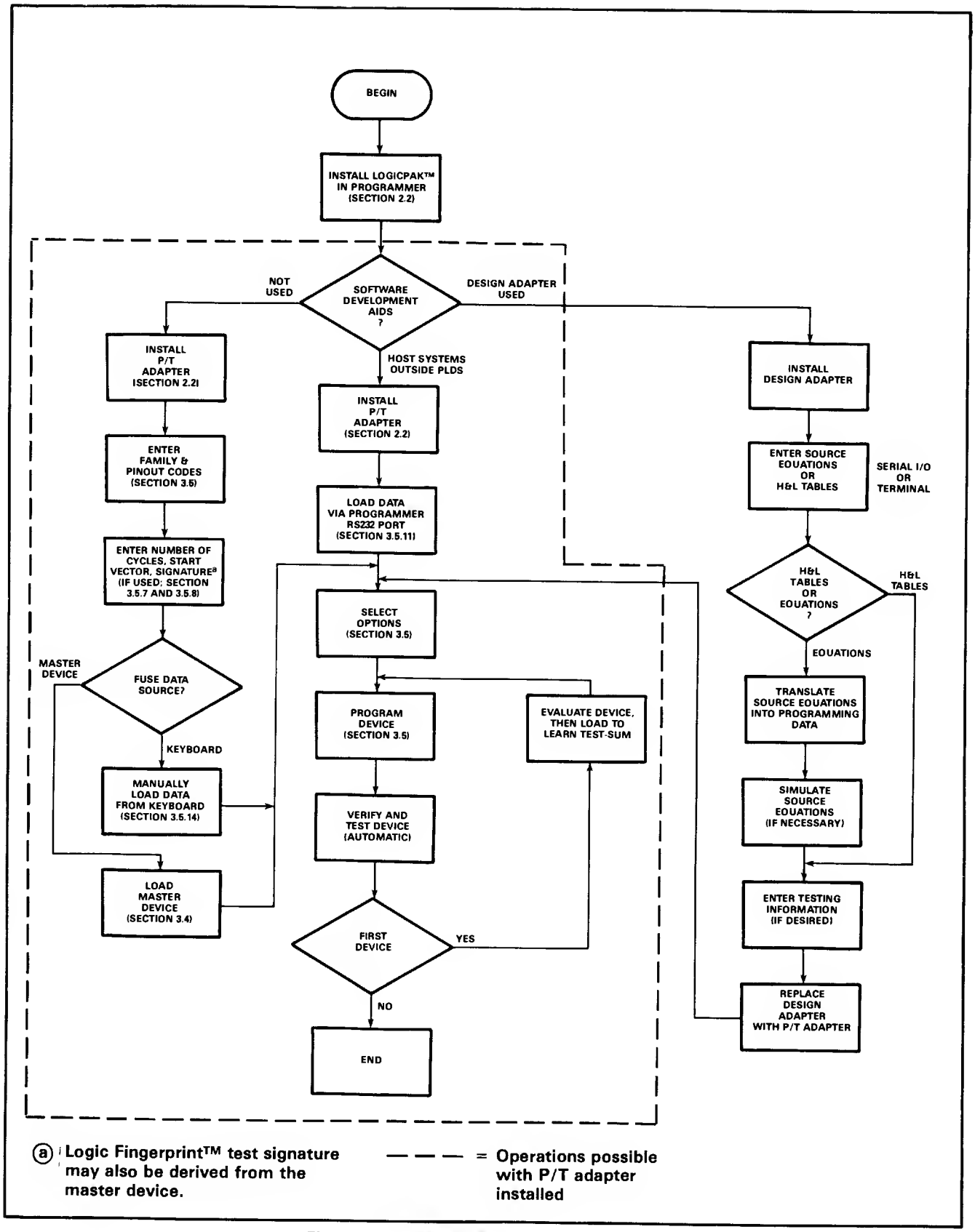
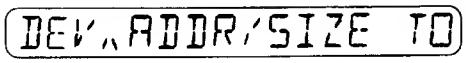


Figure 3-5. Operational Overview Flowchart

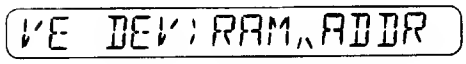
2. 

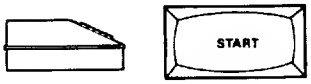
29A Displays



3. 

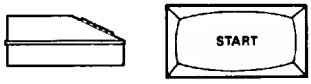
29A Displays



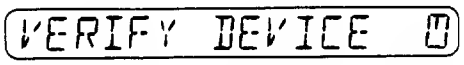
4. 

29A Displays

5. Enter the family code and pinout code (see section 3.4.1) if necessary.
6. Insert the device to be verified and/or tested into the LogicPak™ (see section 3.4.2).

7. 

29A Displays



NOTE

XXXX is the sum-check.

8. Remove the master device from the adapter socket (see section 3.4.3).

To verify and test a device from terminal control, follow the steps given below.

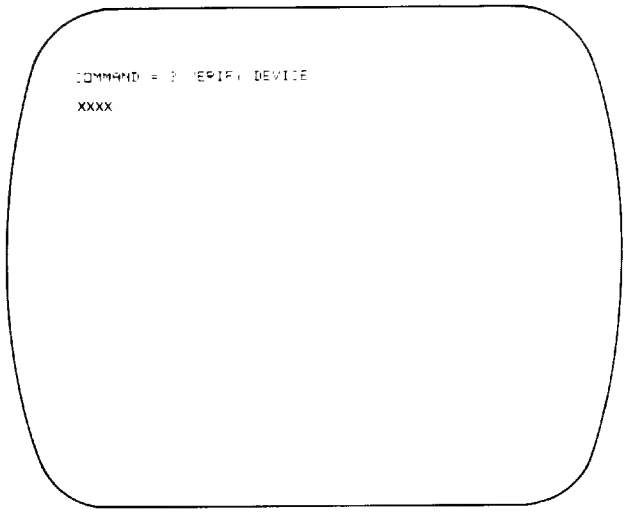
1. Place the system in the terminal mode; see section 3.5.1.
2. Enter the family and pinout codes, if prompted by the terminal.

NOTE

If options are desired (see section 3.5), select options and parameters as needed before proceeding.

3. 

Terminal Displays



There will be a short delay after pressing 3. This is when the programmer is verifying and functionally testing the device. If no errors occur, the terminal displays XXXX.

NOTE

XXXX is the sum-check of the device fuses.

3.5 SYSTEM COMMANDS

In addition to the copy (load or program), verify, edit, and select functions described in the Operation Section of your programmer manual, the LogicPak™ offers numerous system commands that allow you to manipulate data and set parameters. System commands are accessed by entering a two-character select code from the programmer front panel or a one-character menu code from the terminal. Some commands will prompt for a data entry. The operational overview (figure 3-5) will help you develop data and program a device using the system commands and programmer operations. Table 3-1 lists the select codes for Data I/O programmers to enter system commands from the programmer front panel or from a terminal in terminal mode.

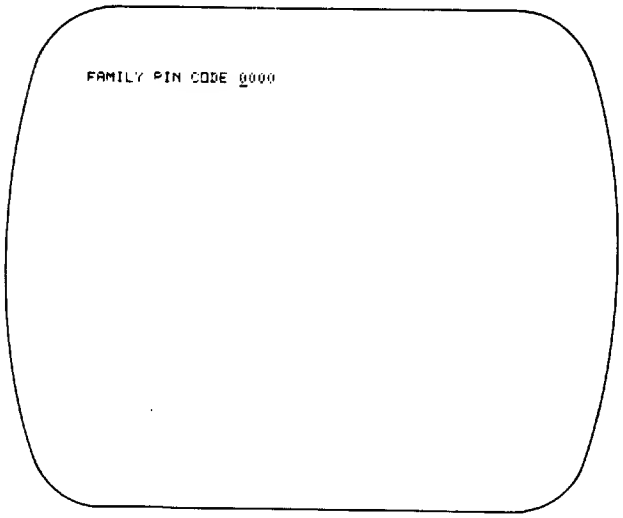
NOTE

The sequence explanations assume no operating errors. If these occur, the programmer signals audibly (except in remote control) and displays a two-digit error code. It also beeps once when an incorrect key is pressed. Error codes are explained in section 4.1 (table 4-2) and in your programmer manual. Some errors will return you to the programmer front panel control.

3.5.1 ENABLE TERMINAL MODE

Select code E1 transfers control of the PLDS to the terminal. After control is transferred, the 29A will display only its action symbol. This command allows you to access data development and remote operations resident in the design adapters and remote operations using the P/T adapters.

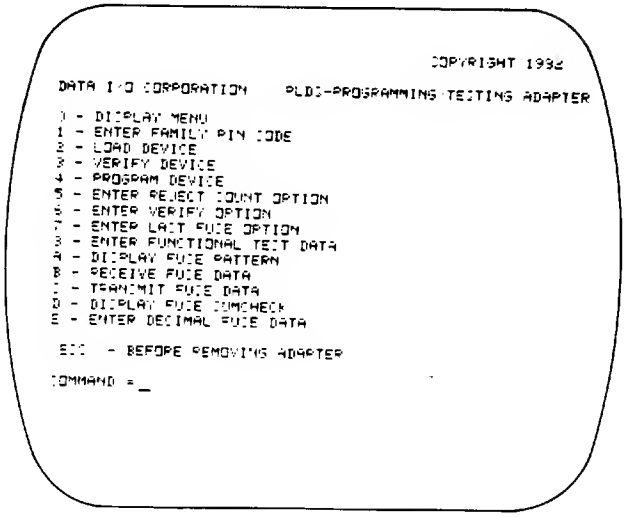
The terminal will prompt you to enter a family pinout code unless one has been entered. The terminal will display:



If desired, enter the family and pinout codes; see section 3.4.1. Once the codes have been entered, the terminal will display the command menu; see section 3.5.2. Bypass the entry of these codes by pressing RETURN.

3.5.2 DISPLAY COMMAND MENU

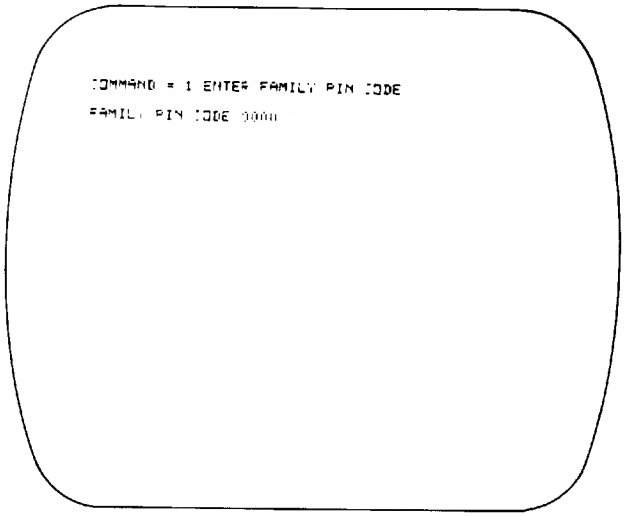
This command causes the PLDS to display its command menu on the terminal, as shown below:



3.5.3 FAMILY CODE AND PINOUT CODE

From the 29A front panel control, family and pinout code entry is part of a device-related operation; see sections 3.4.1 and 3.4.4.

Terminal Displays

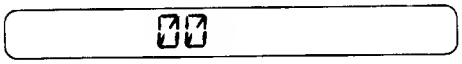


Enter the family and pinout codes. See section 3.4.1 for more detail.

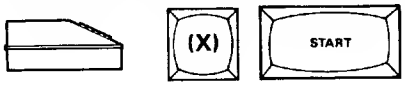
3.5.4 SET REJECT COUNT OPTION

This command allows you to select the number of programming pulses applied to the device fuses before the programmer rejects the device as unprogrammable. The default value of 00 selects the manufacturer's specified number of programming pulses. Refer to the timing diagrams for specific entries to select optional reject values for single-pulse, military, etc., programming specifications.

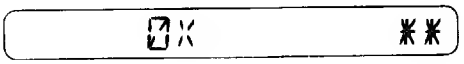
29A Displays

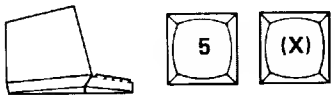


To change the reject count to an optional value, enter the code number (X) specified in the timing diagram.



29A Displays





Terminal Displays

3.5.5 SELECT VERIFY OPTION

Three options are available for selecting verify and functional test routines. These routines are described in detail in section 3.4.6.

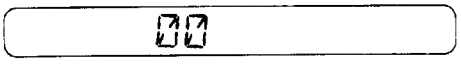
Options available are:

OPTIONS	DESCRIPTION
0	Default option. Perform fuse verify, followed by structured test (if test vectors are present in RAM), and Logic Fingerprint™ test (if one or more Logic Fingerprint™ test cycles are selected), in that order.
1	Perform fuse verify only.
2	Perform structured test and Logic Fingerprint™ test only, in that order. Does not perform fuse verify.

Option 0 (default) is the option used in normal operation. Option 1 checks the programming of the device fuses without checking its functionality. Use option 2 to functionally test devices with the security fuse blown. In addition, option 2 can be used to learn the Logic Fingerprint™ test-sum of a device with the security fuses blown. Fuse data in RAM will be cleared during this operation. Programming cannot occur with option 2 selected.

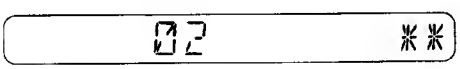
Test options must be entered from the programmer's keyboard or a terminal. The option will remain in effect until it is changed or until the unit is powered down. To reselect the default, key in option 0.

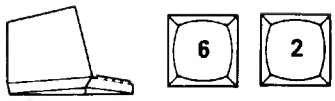
29A Displays



For example, to select functional test only:

29A Displays





Terminal Displays

3.5.6 SELECT SECURITY FUSE OPTION

Some logic devices are equipped with protective fuses called security fuses. Once the security fuses are programmed, the fuse states in the logic array cannot be copied. Programming the security fuses makes it very difficult to pirate a device design.

The PLDS security fuse programming feature is a fail-safe function. You can either enable programming of the security fuse at all times, only allow programming when security fuse data are downloaded to the PLDS via the serial port, or disable programming completely, whether security fuse data are downloaded or not.

When the security fuse has been blown, a Logic Fingerprint™ test and structured test can still be performed, but a fuse verify operation is not possible. See section 3.5.5.

To enable programming of security fuses two conditions must be met: 1) the security fuse state in the programmer RAM must be 1 (or true), and 2) security fuse programming must be enabled. Once the security fuse option is selected, it will remain in effect until changed or until the programmer is turned off.

When security fuse data are entered into RAM manually or in the JEDEC ASCII-logic format, data in the G field indicate the state of the security fuse. The G field does not affect the enable state of the security fuse option; the enable state must be entered separately. This can be done before or after loading JEDEC ASCII-logic format data.

Security fuse states cannot be loaded from a master device.

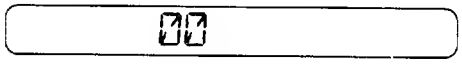
CAUTION

Once the security fuse is programmed, you can no longer verify the state of any fuse in the device. The process cannot be reversed; therefore, be certain that you want to program the security fuse before you activate this function.

Security fuse select-code options are:

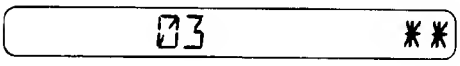
OPTION	DESCRIPTION
0	Default option. Disable programming and set the security fuse state in RAM to 0.
1	Disable programming, and set security fuse state in RAM to 1 (true).
2	Enable programming, and set security fuse state in RAM to 0. (Data downloaded in the JEDEC format can change the security fuse state to 1.)
3	Enable programming, and set security fuse state in RAM to 1. (Data downloaded in the JEDEC format can change the security fuse bit back to 0.)

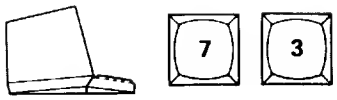
29A Displays



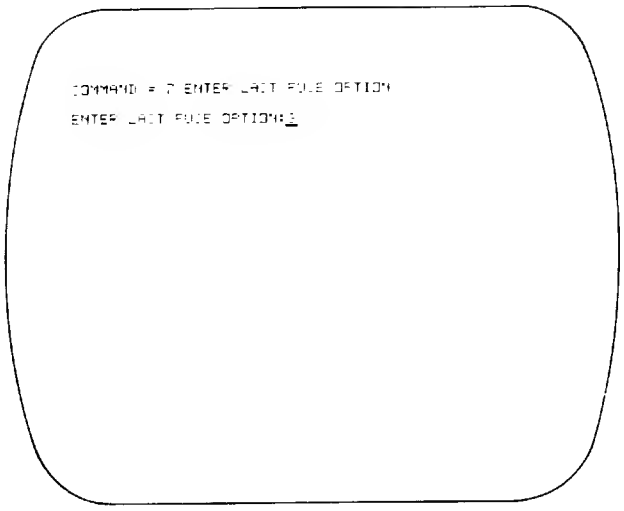
For example, to enable security fuse programming and set security fuse state in RAM to 1 (option 3):

29A displays





Terminal Displays

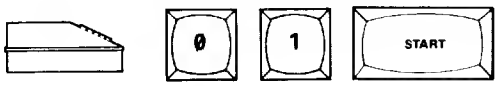


3.5.7 SET NUMBER OF LOGIC FINGERPRINT™ TEST CYCLES

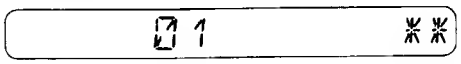
This command allows you to select the number of test cycles that are performed during the Logic Fingerprint™ test. See section 1.4.3 of the LogicPak™ manual for a full description of this test. The default value is 00, which disables the Logic Fingerprint™ test.

29A Displays

For example, to enable one cycle of testing,

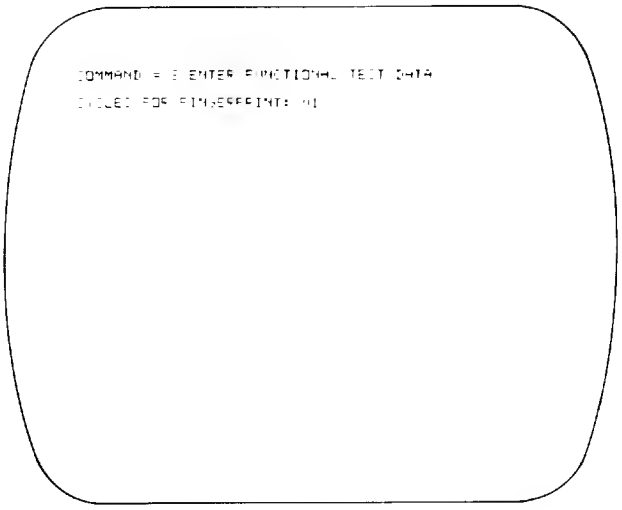


29A Displays



and enter the number of cycles desired.

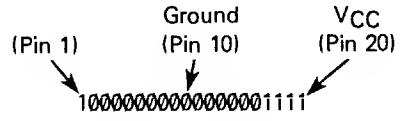
Terminal Displays



3.5.8 ENTER LOGIC FINGERPRINT™ TEST STARTING VECTOR

This command enables you to view or enter the starting test vector and resulting test-sum for the Logic Fingerprint™ test.

For this example we will use an arbitrary starting vector for a 20-pin device of:



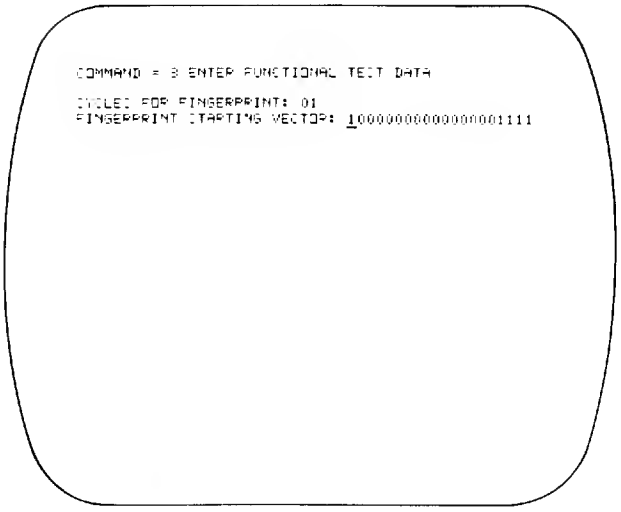
NOTE

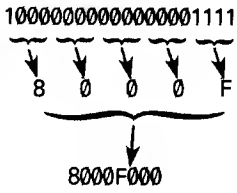
A "1" represents a high; a "0" represents a low to be applied to a particular device pin.

Values entered for ground and V_{CC} are included and affect the test-sum, but have no effect on the device under test. Values entered for dedicated clock and output-enable pins on registered parts must be entered as either 0 or 1. However, they have no effect on the device under test.

Terminal mode allows the starting vector to be entered bit-by-bit after entering the number of cycles for the Logic Fingerprint™ test. For programmer front panel operation, the vector must be represented by hexadecimal numbers as shown on the following page.

Terminal Displays





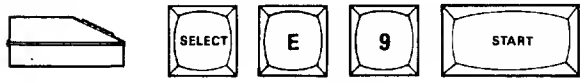
Starting vector (binary)

(hexadecimal)

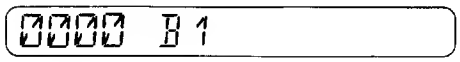
Starting vector (hexadecimal)

The unused portion of the 32-bit vector is assumed to be zeroes and must be included in the hexadecimal vector entry.

For example:



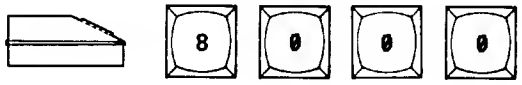
29A Displays



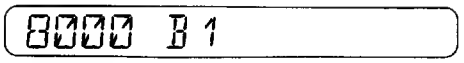
NOTE

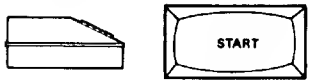
The eight-character starting vector is entered into the programmer in two fields. B1 identifies the first field.

To enter the first four hexadecimal digits,

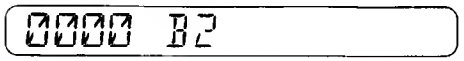


29A Displays



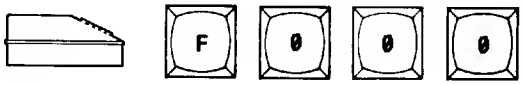


29A Displays

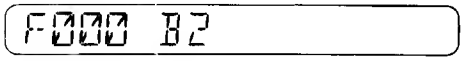


B2 represents the second field.

Enter the remaining hexadecimal digit by pressing



29A Displays

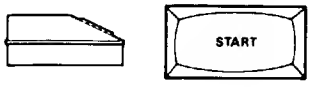


The zeroes are ignored, but are needed to correctly position the "F."

Assume that this vector, when applied to a logic device, gives the following test-sum in hexadecimal:

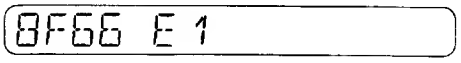
8F66FDAF

The E1 field represents the first four characters of the test-sum. These can be viewed or entered at this time.

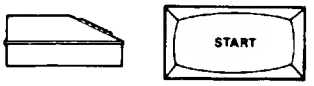


Enter the first four characters of the test-sum.

29A Displays

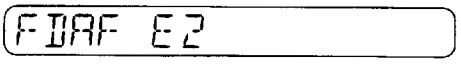


To view or enter the next four characters (E2 field)

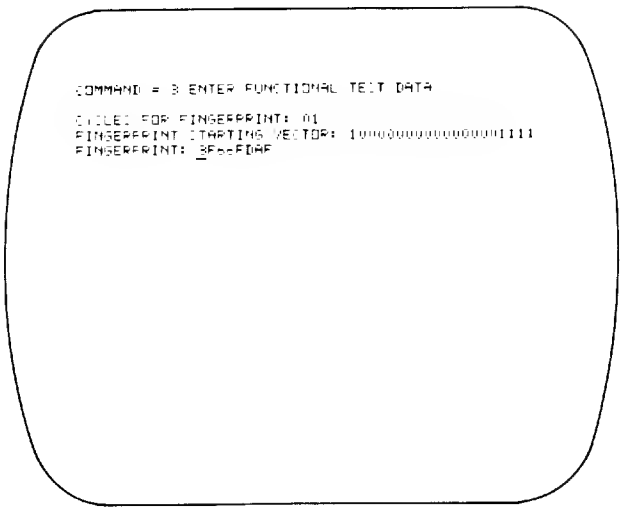


Enter the next four characters.

29A Displays



Terminal Displays



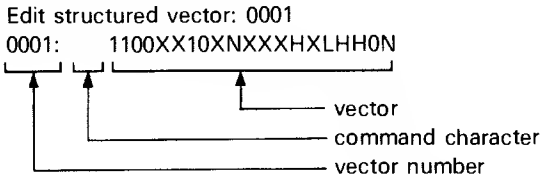
3.5.9 ENTER STRUCTURED TEST VECTORS

After the Logic Fingerprint™test parameters are entered, the terminal entry of structured test vectors can begin. Structured test vectors cannot be entered from the programmer front panel. (See section 1.4.3 and appendix A for a detailed explanation of structured tests.)

Vectors are created by downloading JEDEC 'V' fields, simulating a source file containing a function table, or by using the vector editor.

When the Logic Fingerprint™ test information has been entered (or skipped by entering *RETURN*, the vector editor menu appears (see figure 3-6), and a prompt appears for the vector number to be edited. The default vector is 0001, as shown in figure 3-6.

The vector editor is a fixed-format line editor with the first column of the displayed line reserved for command characters, as shown below.




```
Command :  8 - Enter functional test data
Cycles for Fingerprint: 01
Fingerprint starting vector: 10000000000000001111
Fingerprint: ED37A9E4

           - DISPLAY -                          - EDITING COMMANDS -
0 ------------- Display menu              D ------- Delete (Kill) current vector
Return -------- Go to next vector         R ------- Repeat current vector
U ------------- Up (previous vector)      CTRL Z -- Exit vector editor
#(N) ---------- Go to vector (N)
Space --------- Move cursor right
BKSP (CTRL H) - Move cursor left
CTRL Z -------- Exit vector editor

Edit structured vector:  0000
0001:  1100XX10XNXXXHXLHH0N
0002:  --------------------
```

Figure 3-6. Entering Functional Test Data

Table 3-2. Vector Editor Command Characters

COMMAND	DESCRIPTION	ACTIVITY
0 (zero)	Display menu	Redisplays menu and restarts editing on the same vector.
U	Up (previous vector)	Moves editing to the next lower vector number (the vector one 'up' on the screen).
#(N)	Go to vector (N)	Entering a '#' in the command column causes the vector editor to prompt for the desired vector number (default = 0001). Entering a vector number greater than the last vector will move you to the last vector.
D	Delete current vector	Current vector is deleted, and all higher vectors moved down one. Current vector number is redisplayed with new vector.
R	Repeat current vector	Creates a copy of the current vector immediately following the current vector. The copy is displayed, with its vector number (one greater than the original). This command may be given for any vector, and existing vectors will be moved to accommodate the new copy.

A character entered in the first column (normally blank) is interpreted as a command and acted upon immediately; otherwise, vector editing is not processed until a *RETURN* is entered (at any point on the line). The command characters recognized in the first column are 0, U, #, D, and R; see table 3-2 for command character definitions.

During operation, the vector editor copies the selected vector to a temporary buffer where all editing changes are made. Then, when a *RETURN* command is entered, the temporary buffer is examined for legal characters before copying back to vector memory. You are not allowed to proceed to another vector until all characters are legal in the current vector. Typing A *CTRL Z* to exit the vector editor will leave the selected vector in its original state.

An "empty vector" is represented by a dash in all pin positions. This will appear as the first vector in an empty vector editor buffer, or as one past the last vector where data are present in memory. All vectors are numbered lower than the empty vector.

To edit a vector, follow the steps below.

1. Move the cursor foward (using the spacebar) and backward (using the backspace) along the displayed vector until it is positioned over the test condition to be changed.
2. Type the desired test symbol to enter it into the vector image; the allowable test conditions are 0-9, X, N, F, H, L, Z, C, P, and K (see table 3-3 for test symbol definition).

NOTE

"X" is not defined in the JEDEC format. The "X" is treated as an "N" for outputs and leaves an input at its previously defined state.

Table 3-3. Vector Symbol Definition

VECTOR SYMBOL	DEFINITION
0	Drive input low
1	Drive input high
2-9	Drive input to supervoltage #2-9
C	Drive input low, high, low
K	Drive input high, low, high
N	Power pins and outputs not tested
L	Test output low
H	Test output high
Z	Test output for high impedance
F	Float input or output
X	Ignore input or output (not defined in JEDEC format)
P	Preload (applied to clock pin)

Test conditions 2 through 9 specify non-TTL levels (supervoltages) that access special device features. A device may be damaged by improper use of supervoltages.

3. Enter *RETURN* or *CTRL Z* at any point to move to the next vector or to exit the vector editor.

CAUTION

All devices listed in Table 1-2 with Logic Fingerprint™ Limitation 3 may fail structured test vectors if the same precautions listed under Limitation 3 of section 1.3 are taken. This limitation occurs because these registered devices will not power up in the same state every time the test is performed and because these parts do not possess the preload capabilities discussed later in this section.

Register Preload. In some registered logic devices, the internal registers can be arbitrarily loaded to a desired state. This capability allows easier functional testing by providing a means of achieving states which may be difficult or impossible to enter by normal state transitions.

For devices which have the register preload feature (see table 3-4) preload is accomplished by using a "preload vector," a structured vector which has a "P" symbol in the clock pin position. Also in the preload vector are special symbols in the positions of the pins associated with loading of the registers. The symbols used in the preload vector and their functions are described in table 3-5.

Table 3-4. Preloadable Devices

PAL20R4A
PAL20R6A
PAL20R8A
TIBPALR19R4
TIBPALR19R6
TIBPALR19R8
TIBPALT19R4
TIBPALT19R6
TIBPALT19R8

All pins not used in the device's preload algorithm (regardless of the symbol placed in the preload vector pin position) are treated as "X"s (left in their previous state). Pins which are used in the preload algorithm may not return to their original state following preload. For example, to preload a 20-pin device with preload pins (most likely device outputs) 12 through 19, you might apply the following preload vector: (clock pin assumed to be pin 1).

0001: PXXXXXXXXNXHLHLHLHLN

When the preload vector is applied during functional testing, the device-specific preload algorithm is invoked and the registers are loaded with the appropriate data to make the outputs high ("H") or low ("L"). The output pins are then tested to verify that the preload was successful.

Table 3-5. Preload Vector Symbols

P	Identifies preload vector and invokes preload algorithm. (Allowed on clock pin only; otherwise treated as "X".)
Ø	Preloads a logic "Ø" into the register $\overline{Q}$ output, meaning a logic "I" will be loaded into the register Q output. Does not test device outputs.
1	Preloads a logic "1" into the register $\overline{Q}$ output, meaning a logic "Ø" will be loaded into the register Q output. Does not test device outputs.
L	Preloads register with the appropriate level such that a logic "Ø" appears on the device output pin. Also tests the preloaded device output and indicates an error if a logic "Ø" is not found.
H	Preloads register with the appropriate level such that a logic "1" appears on the device output pin. Also tests the preloaded device output and indicates an error if a logic "1" is not found.

Assuming the device has an inverter between the register output and the output pin, another method of achieving the same results as above is to use the following two vectors:

0001: PXXXXXXXXXNX1010101010N
0002: XXXXXXXXXNQHLHLHLHLN

The first vector is a preload vector using "1"s and "0"s to load the $\overline{Q}$ output of the register with the data indicated (thus making the Q outputs of the registers the complements of the data in the vector). Since we have assumed an inverter between the Q output and the output pin, the data found on the output pins after execution of the preload vector should reflect the "1"s and "0"s in the preload vector. The second vector shown is a conventional structured vector which tests the outputs for the desired data.

The "1" and "0" preload symbols are most useful for preloading registers whose state cannot be read at a device pin, or for any case in which the user is concerned with setting up the state of the REGISTERS and not necessarily the state of the output pins.

The "H" and "L" preload symbols are used to preload the states of OUTPUT PINS whose states are determined by the data in internal registers. The programming/testing adapter firmware determines what data should be placed in the internal registers to provide the correct outputs. Users concerned with preloading the state of the internal registers can use the "H/L" preload vector to load and automatically verify internal register states provided that data inversion (if any) between registers and outputs is considered.

3.5.10 DISPLAY FUSE PATTERN

This command outputs the fuse pattern in the programmer data RAM to the serial port of the programmer. The fuse states are a series of 1s and 0s representing whether a fuse is blown (1) or left intact (0). Each fuse can be identified by a decimal number (figure 3-7). The fuse states are arranged in a matrix that corresponds to the logic diagram of the device. This is useful for transferring a fuse pattern to a logic diagram for documenting a device fuse pattern. See figures 3-7 and 3-8.

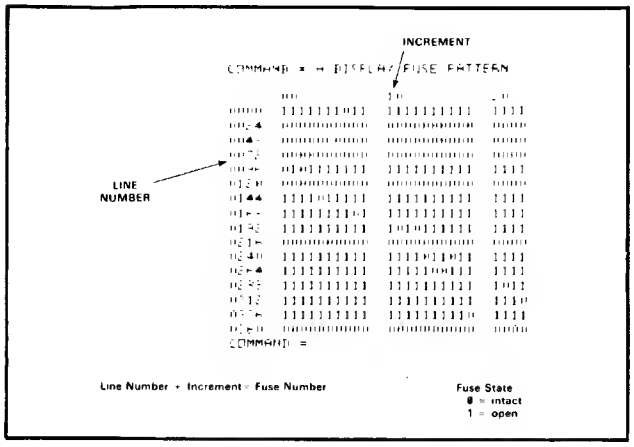
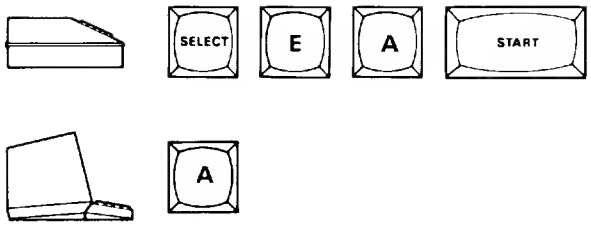
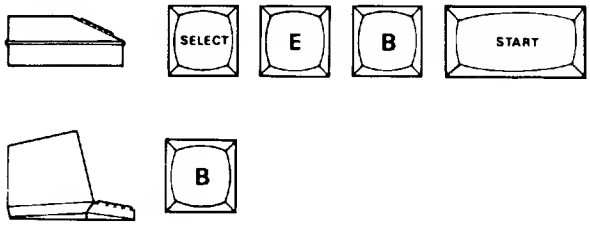


Figure 3-7. Fuse Pattern



3.5.11 RECEIVE FUSE DATA

This command prepares the programmer to receive fuse data from a peripheral via the programmer serial port in the JEDEC standard ASCII-logic format (LogicPak™ manual, appendix A).



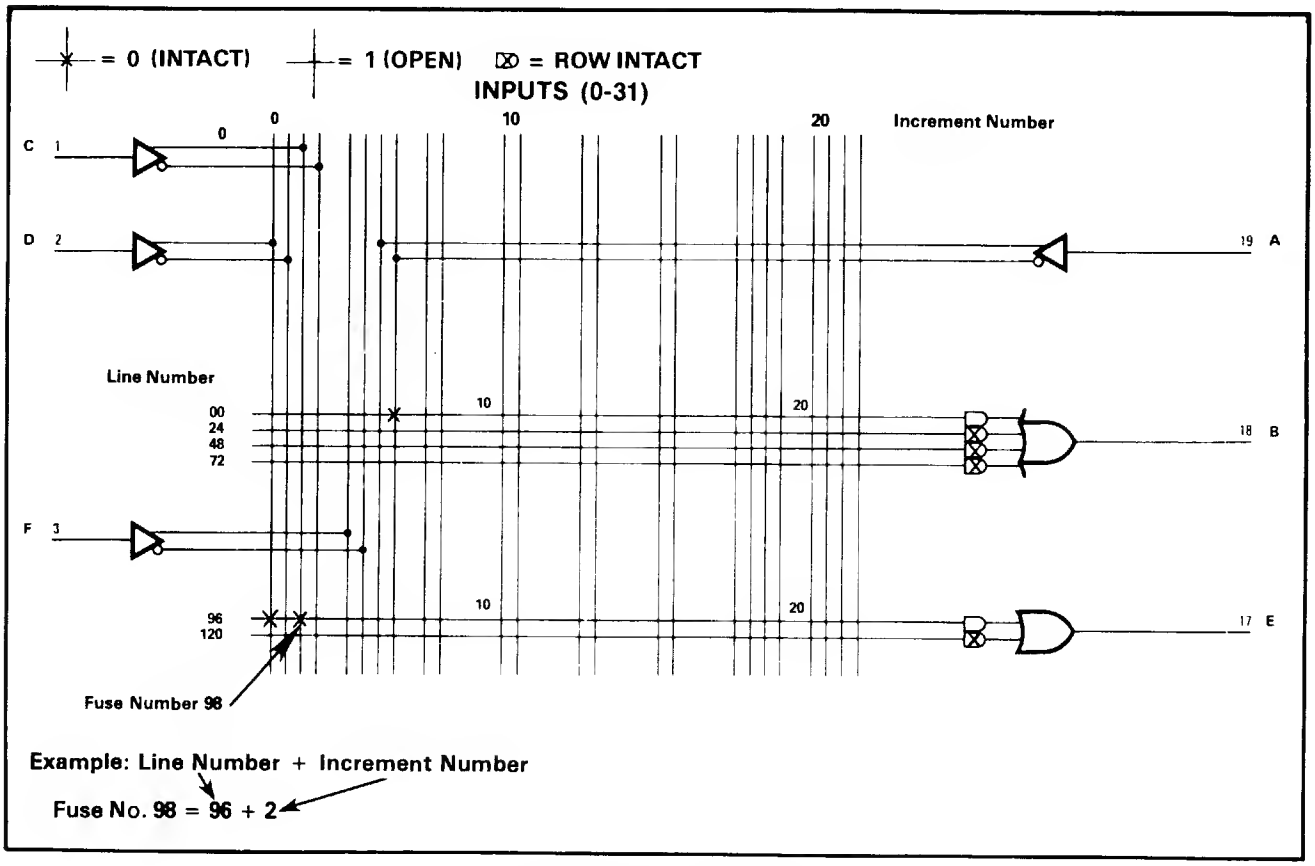
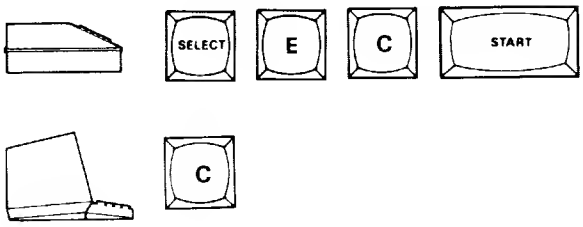


Figure 3-8. Logic Diagram

3.5.12 TRANSMIT FUSE DATA

This command prepares the programmer to output fuse data via the serial port in the JEDEC ASCII-logic format (appendix A). See Figure 3-9.



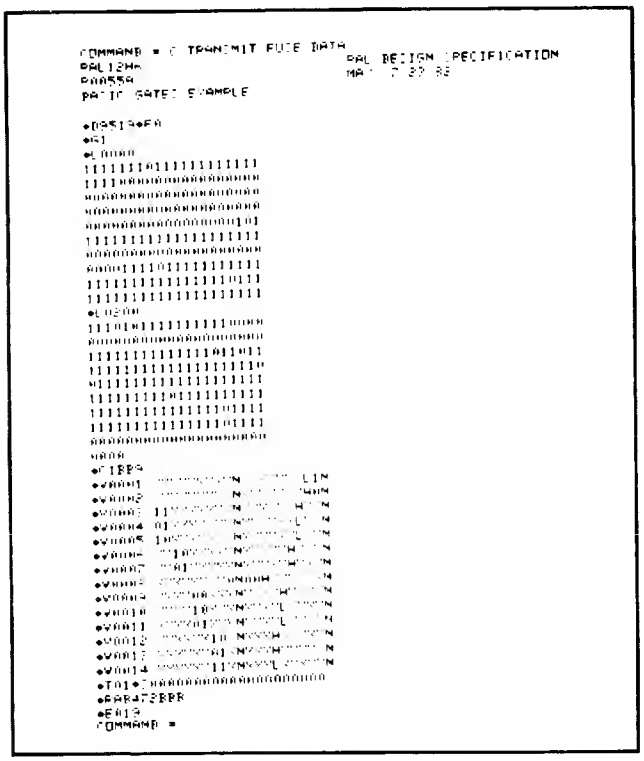
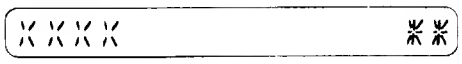


Figure 3-9. Sample Printout of JEDEC Format

3.5.13 DISPLAY SUM-CHECK OF FUSE DATA

This command displays the sum-check of the fuse states in the programmer data RAM (the C field in the JEDEC format). The sum-check should match one from a previously programmed device that is known-good.

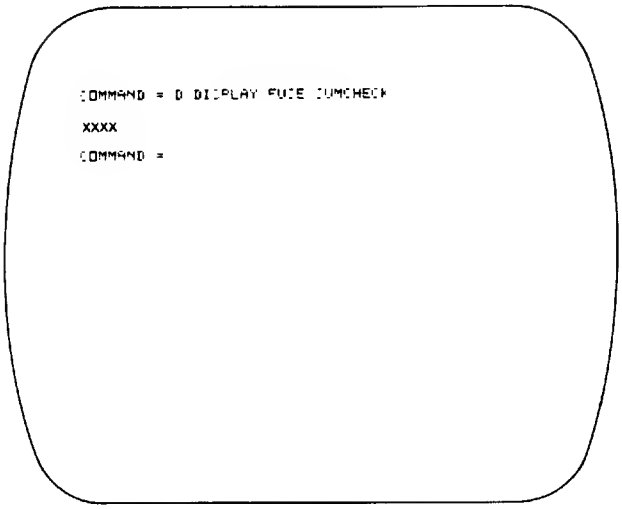
29A Displays



NOTE

XXXX is the fuse array sum-check of the device.

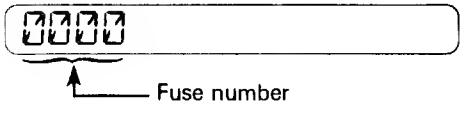
Terminal Displays



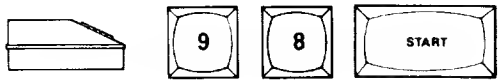
3.5.14 ENTER FUSE NUMBER AND STATE

Programming information in RAM for the logic device fuses may be entered using this command. Refer to figure 3-6 for an example of the fuse states by fuse numbers. A fuse number is obtained by adding the line number and increment number corresponding to the intersection where the fuse is located. (See figure 3-10.)

29A Displays



Enter a decimal fuse number; for example, 98.



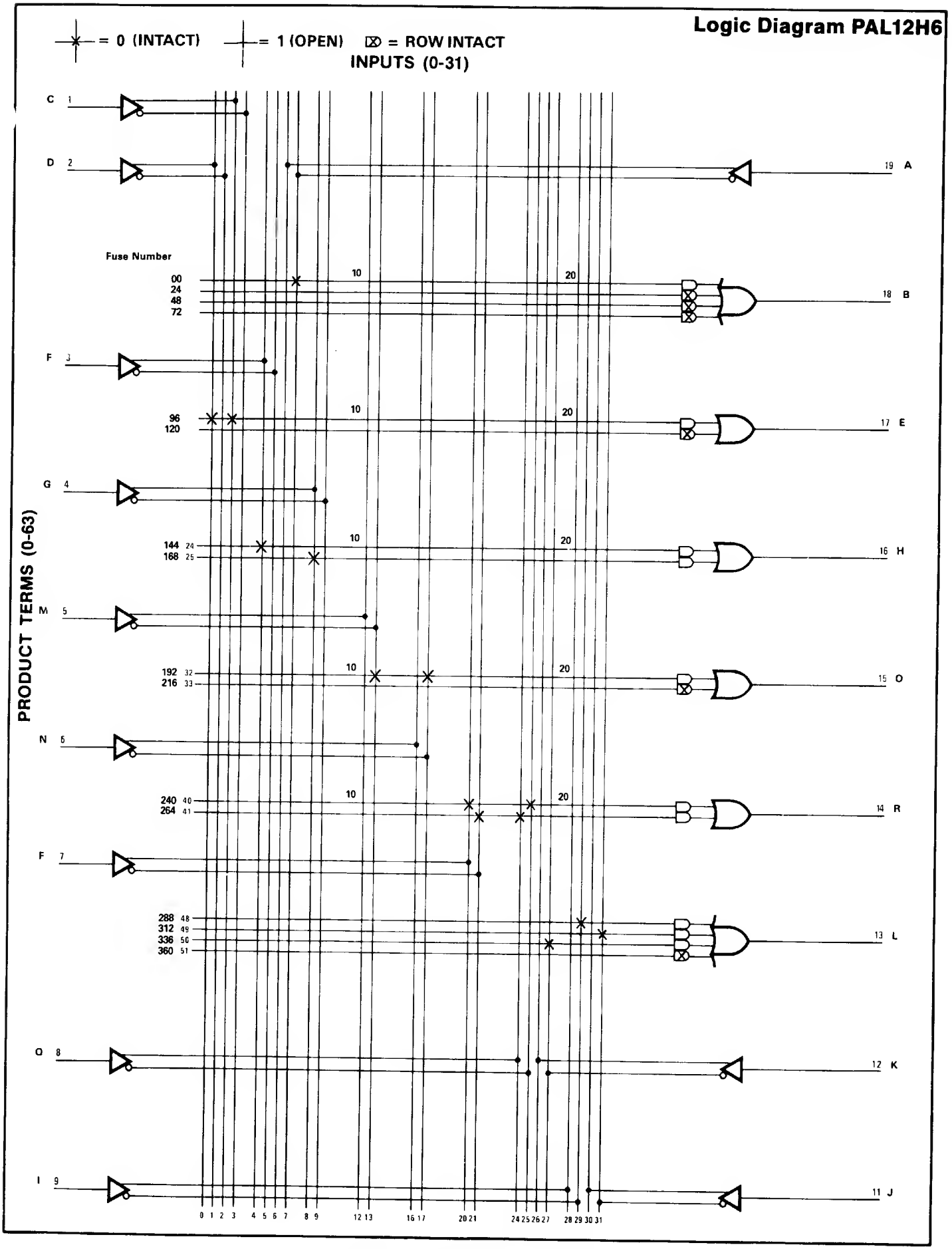
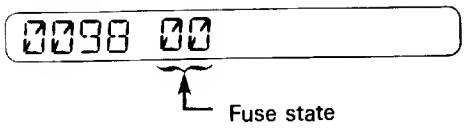
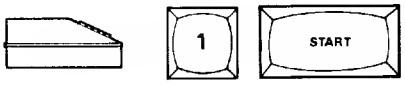


Figure 3-10. Complete Logic Diagram

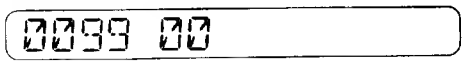
29A Displays



This display indicates that RAM data for fuse 98 is set for "don't program." To change it to a program state:



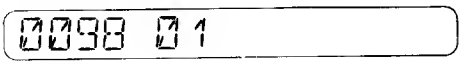
29A Displays

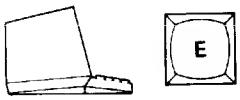


(Fuse number increments automatically.)

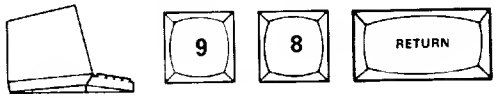
To decrement a fuse number:

29A Displays

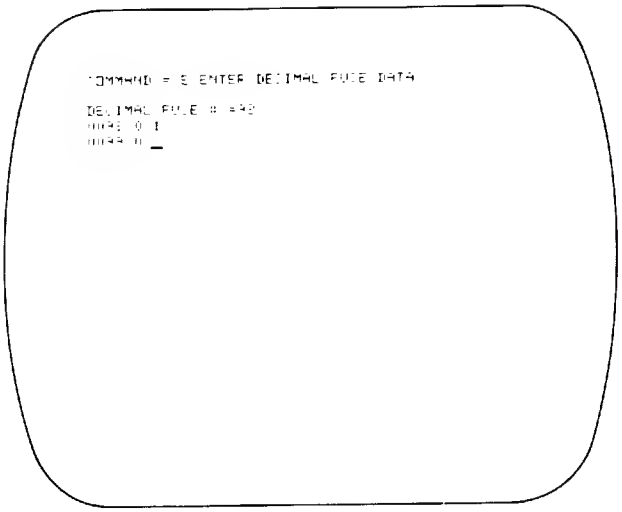




Enter the fuse number; for example, 98.

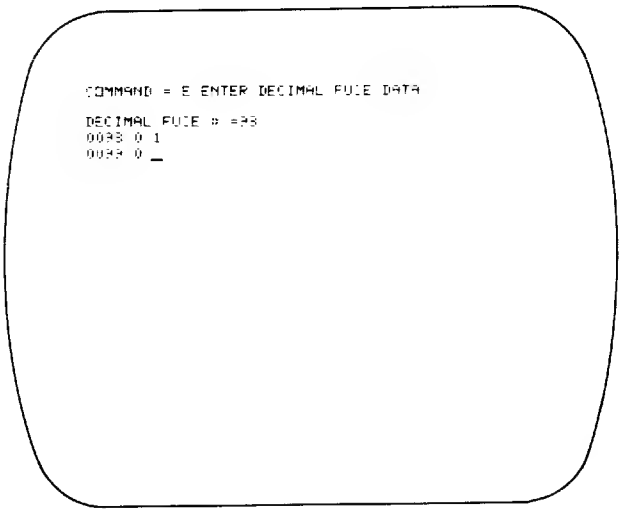


Terminal Displays



This display indicates that RAM data for fuse 98 is set for "don't program." To change to a program state:

Terminal Displays



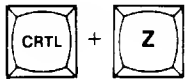
This indicates that fuse 98 will program, increments the fuse number display, and indicates the state of fuse 99 in RAM. To display the next fuse,

To display the previous fuse,

To jump to a new fuse location,

then the decimal fuse number

or



simultaneously to exit the edit mode.

3.5.15 DISPLAY CONFIGURATION NUMBER

This command displays the configuration number of the adapter firmware. Configuration numbers are used as serial numbers for firmware.

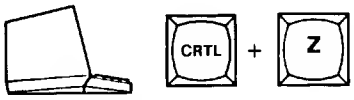
29A Displays

NOTE

XXXX is the configuration number of the firmware in the adapter plugged into the PLDS.

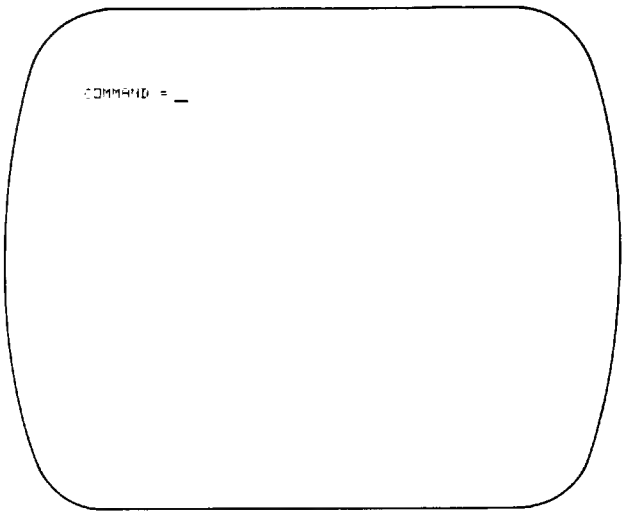
3.5.16 EXIT COMMAND

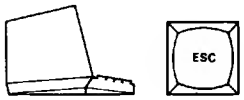
During terminal mode, use this function to exit specific operating modes.



simultaneously

Terminal Displays





returns control to the programmer front panel from terminal control.

SECTION 4
CALIBRATION AND TROUBLESHOOTING

4.1 OVERVIEW

The material in this section is provided to help you keep your LogicPak™ and P/T adapter in optimum operating condition. For users who prefer to do their own calibration, detailed procedures, including measurement charts and timing diagrams (section 4.2) for each device, are provided. The basic procedures to set up the LogicPak™ in the calibration mode are described in section 4.2.

4.2 CALIBRATION

The need for calibration varies with the amount of use your LogicPak™ receives. Generally, we suggest calibration whenever: 1) programming yields fall below the manufacturer's recommended minimums, 2) when troubleshooting has been completed, or 3) if your company policy requires periodic calibration certification. Because the LogicPak™ must be calibrated with an adapter installed and the values vary with different adapters, the detailed calibration procedures, measurement charts, and timing diagrams are provided in each adapter manual. The calibration setup procedure is described in this section.

NOTE

If calibration or repair is required, but you lack the facilities to accomplish it, contact the nearest Data I/O Service Center. Because of the different programmer mainframes and adapters this manual does not attempt to cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak™.

To prepare the LogicPak™ for calibration:

1. Remove the adapter (if any) from the LogicPak™ (see section 2.3).
2. Remove the four phillips-head screws on the top of the LogicPak™ cover (see figure 4-1).
3. Remove the two allen screws on each side of the LogicPak™ cover (see figure 4-1).
4. Lift the cover off the circuit board cage assembly.
5. Plug the adapter into the connector on the pin driver board as shown in figure 4-2.
6. Plug the LogicPak™ into the programmer.

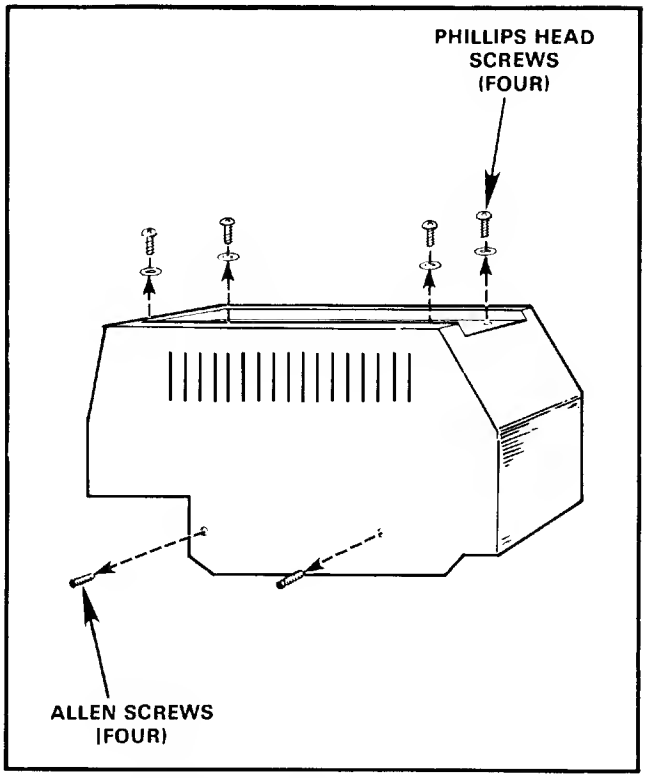


Figure 4-1. LogicPak™ Cover Removal

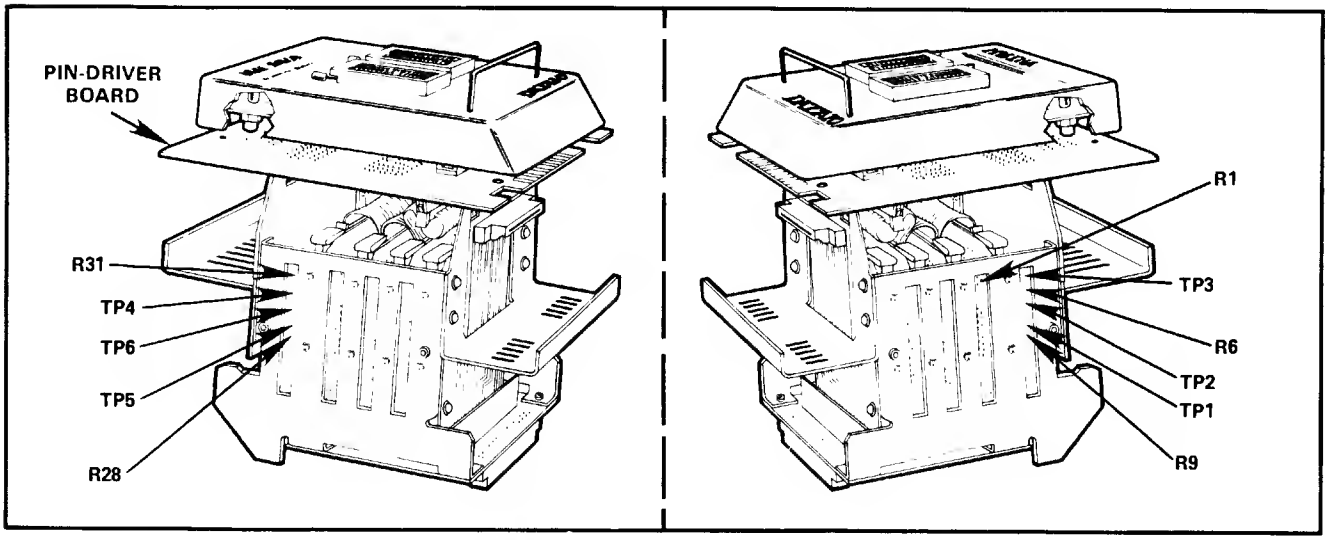


Figure 4-2. Calibration Equipment Setup

Because of the different programmer mainframes, this manual does not cover all areas of programmer calibration. Instead, it lists the steps necessary to calibrate only the LogicPak™ and adapter.

Calibration of the LogicPak™ and adapter consists of three parts:

1. Power supply calibration--measures the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this part of the calibration procedure must be done first. Refer to your programmer manual.
2. DC calibration--consists of measuring and adjusting critical DC voltage levels generated by the LogicPak™.
3. Waveform observation--enables observation of waveforms on an oscilloscope to ensure compliance with the device manufacturers' critical voltage and timing specifications.

Because the first part of the calibration procedure (power supply calibration) varies with the type of programmer you have, this manual refers you to your programmer manual for details on power supply calibration. DC calibration is discussed in section 4.2.1 and waveform observation is detailed in section 4.2.2. For information on how to carry out these steps on various programmers, consult your programmer manual.

The following equipment is necessary to calibrate the LogicPak™:

- Three-and-a-half-digit digital voltmeter (DVM)
- Dual-trace oscilloscope (Tektronix 465 or equivalent)

4.2.1 DC CALIBRATION (Steps 1-10 and 12)

These DC calibration procedures enable you to adjust critical DC voltage levels generated by the LogicPak™. To follow these procedures use the measurement chart at the back of this section (table 4-3), which contains the information necessary for all DC calibration tests. This information is included on the measurement chart in columns with the following headings:

- Step No.--tells which step to use for each test. Step numbers are set at the programmer keyboard and reflected in the display.
- Test No.--identifies individual tests.
- Test description--identifies the functions being tested.
- Measurement location--tells which socket pins or circuit board test points to probe for measuring voltages.
- Measurement--specifies allowable measurement ranges. If a reading falls outside the range and you cannot adjust it to within the range, do not use the LogicPak™ until the problem is corrected.
- Adjustment location--tells which potentiometer to adjust if a measurement is out of range.
- Comments--gives special instructions for particular tests.

The DC calibration procedures follow:

CAUTION

Remove all devices from the sockets before entering the calibration mode (see section 3.4.3 for details). Calibration voltages may damage any device in the LogicPak™ sockets.

1. Turn the programmer power on.
2. Put the programmer into the calibration mode by following the key sequences in table 4-1. The table also explains how to increment, decrement step 2, and how to enter calibration at an advanced step (which is required during the waveform calibration part of the process).
3. Perform the general calibration steps (steps 1-10 and 16) on the measurement chart.

Table 4-1. Key Sequence to Access the Calibration Mode

Programmer System	Key Sequence to Enter Calibration Mode	Increment Step No.	Decrement Step No.
19	Press SELECT Press C2 Press ENTER Enter Step Number [a] Press START	Enter	Review
29A	Press SELECT Press C1 Press START Enter Stem Number [a] Press START	Start	Review
100A	Press SELECT Press 12 Enter Step Number [a] Press START	Start	Backspace

[a] Optional

CAUTION

If the LogicPak™ fails the second step on the measurement chart, DO NOT proceed to the next step. The hardware must pass this step or further testing may damage the LogicPak™.

If the LogicPak™ fails any step on the measurement chart, do not continue to the next step. Refer to table 4-2, which lists error codes and descriptions. Subsequent tests will not give valid results unless all preceding steps are passed and adjustments made.

Table 4-2. LogicPak™ Error Codes

ERROR CODE	DESCRIPTION	ACTION
25	No Socket Adapter	Insert appropriate socket adapter.
30	No (or Invalid) Device Selected	Enter valid device family and pinout codes (refer to Comparison Chart of Programmable Logic Device in each adapter manual).
31	Overcurrent	Hardware error in LogicPak™ or shorted device. Substitute a known-good device or consult the troubleshooting section. If error 31 is displayed, caused by V_{CC} overcurrent, code 32 will display because 32 is tested before 31.
32	Backward Device	(1) Device plugged in backward; turn it around. (2) See error 31.
33	Source Buffer Write Error (RAM)	Source equations exceed the available RAM space; therefore, (1) Reduce the equation length to fit available RAM. (2) Add more RAM to system to accommodate the equation length (refer to programmer manual to expand RAM).
35	Source Equation Translation Error	Check equation buffer by connecting terminal to examine the equation buffer. This error code lets the operator know that an error exists in the source equations when the programmer is not controlled by a terminal.
36	Begin RAM Pointer Not = 0000	Refer to programmer manual to reset the begin RAM pointer to zero. This error usually occurs when changing from one programming pak to another.
37	Invalid Device-Related Operation	Verify, program, or other illegal operation was attempted, with a design adapter installed.
38	Calibration Step Error	Indicates that you've selected an incorrect calibration step. The error will also occur if a program operation is attempted prior to exist calibration. (1) Exit the calibration mode (refer to the programmer manual). (2) Reenter the correct calibration step number.
63	RAM Write Error	System RAM failure. Refer to programmer manual or contact Data I/O service representative.
65	Firmware Sum-Check Error	Contact Data I/O service representative. This indicates that the EPROM firmware in the LogicPak™ or adapter may have changed since the unit was shipped. Do not continue operation until the situation is corrected.
70	DAC Error V_{CC}	See section 4.4 (troubleshooting).
71	DAC Error Bit Switch Number 1	See section 4.4.

Table 4-2. Continued

ERROR CODE	DESCRIPTION	ACTION
72	DAC Error Bit Switch Number 2	See section 4.4.
73	DAC Error CE	See section 4.4.
74	Logic Fingerprint™ Test Verify Error	Indicates a Logic Fingerprint™ error. (1) Device passed fuse verify but failed Logic Fingerprint™ Test—defective device. (2) Operator has entered wrong test-sum. (3) Device cannot be tested with Logic Fingerprint™ (refer to p/t adapter manual for the limitations of the Logic Fingerprint™ test).
75	Structured Test Verify Error	(1) The device passed fuse verify but failed structured test—defective device. (2) Check structured test vectors and make sure they are correct. If not, reenter the correct vectors. The vector could be invalid, or the operator may have miskeyed a valid vector.
76	Self-Test Error	Indicates failure in the LogicPak™. Consult section 4.4 (troubleshooting) or contact your Data I/O service representative.
77	Security Fuse Programming Error	(1) Indicates that the security fuse option cannot be programmed in the installed device. (2) There is no security fuse option available for this type of device.
78	No Fuse Verify Set	Indicates you've tried to program the device with the verify-option mode set for 2. The verify option won't allow this. When this error code displays, select E6 and enter Ø or 1, and then you will be allowed 1 program.
82	Checksum Error	Indicates an incorrect transmission data from a peripheral to the serial port, including fuse data, CRs, STX, etc.
84	Sum-Check Error	(1) Indicates an error in the fuse data, or (2) Received fuse data does not match fuse sum-check (C-field error).
91	Fuse Address Error	Indicates an invalid fuse address. Check input and make sure fuse address is four decimal numbers or an otherwise valid address.

For each general calibration step on the measurement chart:

- Take measurement readings at the device sockets or test points indicated in the measurement chart.
- Ground the DVM to pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
- The oscilloscope trigger point is called out on the measurement chart photographs.
- The adjustment potentiometers on the waveform generator and the T/rise comparator card enable you to make adjustments when your measurements do not match the measurement chart; figure 4-3 shows the location of these adjustment points.
- Access each new step by pressing START (or ENTER). The new step number will appear on the display when the LogicPak™ is ready for the next step. To return to a previous test, press the REVIEW (or BACKSPACE) key.

4.2.2 WAVEFORM OBSERVATION

Programming waveforms of your LogicPak™ can be observed with an oscilloscope and compared with the timing diagrams at the end of this section. In this way, timing and magnitude relationships can be measured against known specifications to confirm that the LogicPak™ is performing to the device manufacturer's specifications. When step 15 is called, the waveforms will reflect the programming algorithm for only the fuses to be programmed as specified in RAM. To alter the state of the individual fuses, refer to section 3.5.14, "Enter Fuse Number and State" (select code EE). Because the LogicPak™ generates many waveforms, and all calibration adjustments are accomplished in DC calibration, it is only necessary to observe waveforms for commonly used devices or devices that are presenting yield problems. These measurements can be performed on any device by entering the appropriate family pinout code and fuse number (if appropriate).

During the waveform observation phase of the calibration procedure, your LogicPak™ uses a firmware routine that generates programming and verify waveforms for the data stored in system RAM.

4.2.3 EXPLANATION OF TIMING DIAGRAMS

This manual contains a set of timing diagrams for the TI family of logic devices. The timing diagrams show critical waveforms for a specific device but may be verified for any of the TI devices by entering the appropriate family pinout code before invoking the calibration mode. To use these diagrams and photographs, read the information provided below and refer to the sample timing diagram (figure 4-4).

1. Family Pin Code Number--corresponds to the family pin code number of the device.
2. Waveform Variables--lists the minimum and maximum parameter values; voltage and timing parameters other than those listed in this table are to be considered noncritical with a + / − 10% tolerance.
3. Notes--important information pertaining to a timing diagram.
4. Waveform Names--the manufacturer's reference to the pin being observed.
5. Layout Sequence Number--used as a reference point within each diagram.
6. Delay Time Position--indicates the time from the start of the main sweep to the start of the delay time.

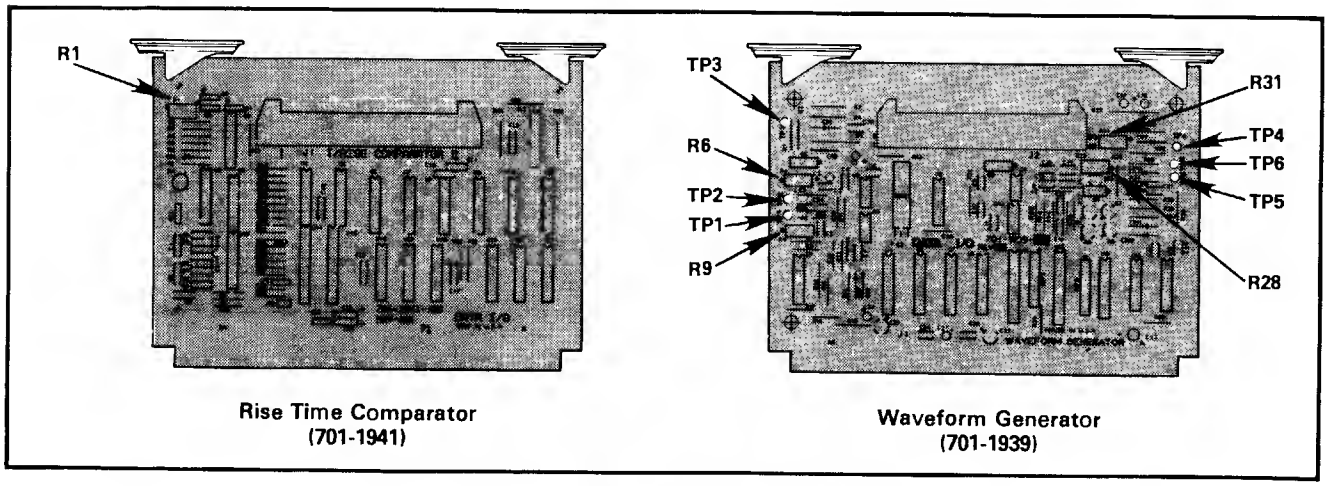


Figure 4-3. LogicPak™ Test and Adjustment Locations

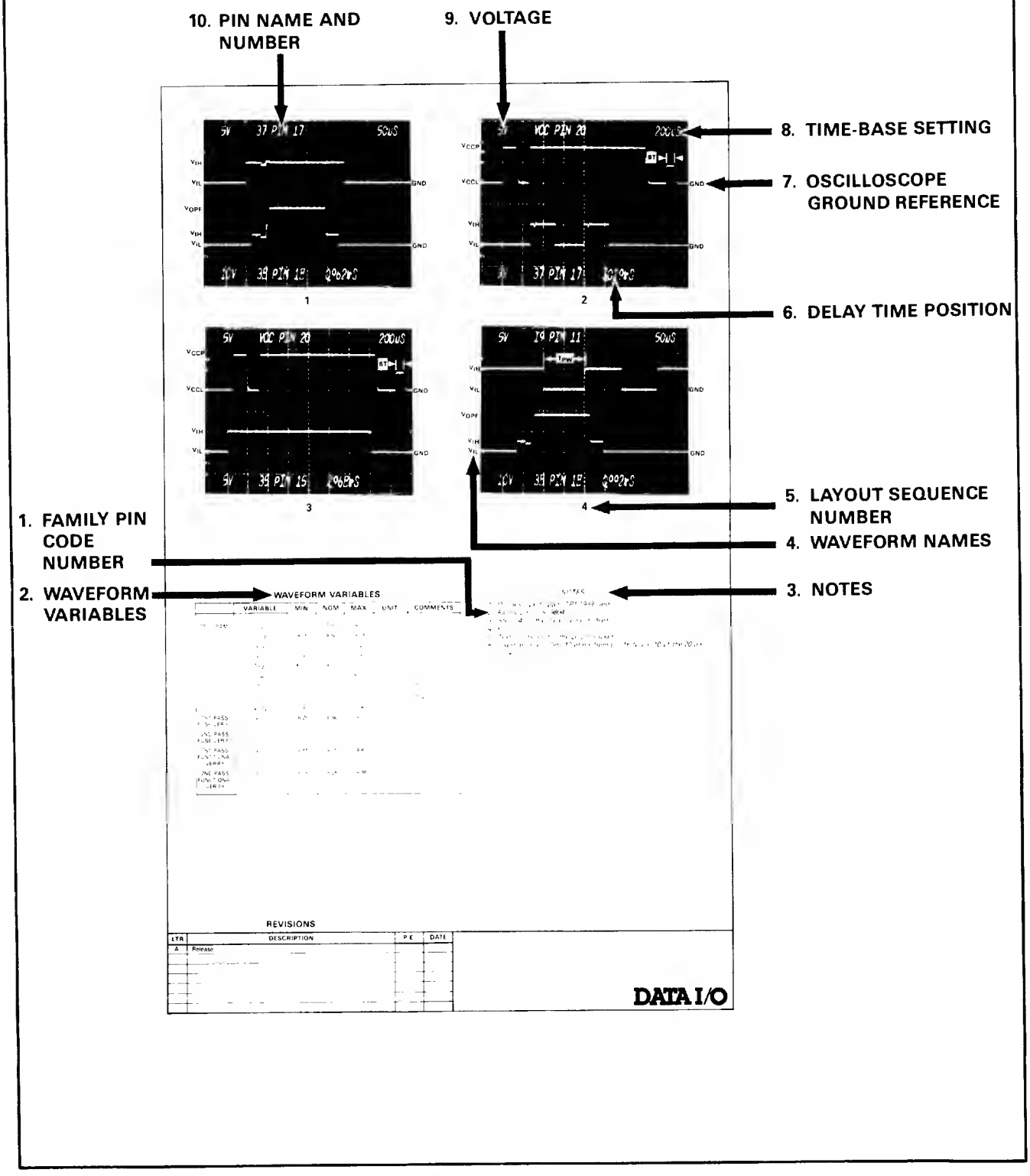


Figure 4-4. Sample Timing Diagram

7. Oscilloscope Ground Reference--ground contact on the socket with its LED illuminated.
8. Time-Base Setting--horizontal positioning of the waveforms is not critical and may vary slightly from the photographs. The important observation is the timing relationship between the waveforms in the photographs. You can adjust this timing relationship on your oscilloscope to set convenient reference points. By considering any time-base variance, you can also make time comparisons between photographs. The time base is always the same for different waveforms in the same photograph.
9. Voltage--indicates volts per division. The one in the upper-left corner is for the top trace and the one in the lower-left corner is for the bottom trace.
10. Pin Name and Number--the device pin name and socket pin number where the waveform can be observed.

Table 4-3. Measurement Chart

REVISIONS

LTR	DESCRIPTION	P E	DATE
A	Release	KM	6/15/88

Measurement Chart for TI PAL Adapter
10-715-1006-001

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
1	1	All pins low	24 pin/all pins	-0.4		0.8		CAUTION[b]
			20 pin/all pins					
2	2	Self-test, sink drivers						See table 4-4 if errors result;
								errors must be corrected to
								continue. Possible errors are
								A0-0F.
3	3	LED test 1						Confirm 24-pin LED on, 20-pin off.
	4	Comparator reference	701-1939/TP5	10.20	10.24	10.28	R29/701-1939	
								CAUTION[c]
	5	V_{CC} supply	24 pin/pin 24	11.9	12.0	12.1	R9/701-1939	Load with 50 5W resistor to
			20 pin/pin 20					ground.[c,d]
	6	CE supply	24 pin/pin 13	19.8	20.0	20.2	R31/701-1939	Load with 100 5W resistor to
								ground.[c,d]
	7	Bit supply SW 1	24 pin/pin 19	19.8	20.0	20.2	R6/701-1939	Load with 100 5W resistor to
								ground.[c,d]
	8	Bit supply SW 2	24 pin/pin 14	19.6		20.4	N/A	Load with 100 5W resistor to
								ground.[c,d]
	9	DAC reference	701-1939/TP6	4.7		5.3	N/A	

CAUTION: DO NOT POWER DOWN AFTER STEP 1.

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]Do not leave programmer unattended in calibration mode beyond step 1.
[c]Insert load resistor after pressing START; remove immediately after performing test.
[d]Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels, refer to step 12.

Table 4-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	KCM	6/15/83

Measurement Chart for TI PAL Adapter
10-715-1006-001

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
4	10	Self-test source drivers						See table 4-4 if errors result.
								Possible errors are E0-FF.[b]
	11	LED test 2						Make sure that the 20-pin socket
								LED is on and 24-pin LED is off.[b]
	12	Socket pins TTL high	24 pin/pins 2,4,6,8,10,13,16,18,19,21,23	3.0		5.2		
			20 pin/pins 2,4,6,8,11,13,15,17,19	3.0		5.2		
	13	Socket pins TTL low	24 pin/pins 1,3,5,7,9,11,14,15,17,20,22	-0.4		0.8		
			20 pin/pins 1,3,5,7,9,12,14,16,18	-0.4		0.8		
5	14	Socket pins TTL low	24 pin/pins 2,4,6,8,10,13,16,18,19,21,23	-0.4		0.8		If error 76 occurs during steps
			20 pin/pins 2,4,6,8,11,13,15,17,19,	-0.4		0.8		5-16, perform steps 2 and/or 4
			LEDs off					for diagnostics.[b]
	15	Socket pins TTL high	24 pin/pins 1,3,5,7,9,11,14,15,17,20,22	3.0		5.2		
			20 pin/pins 1,3,5,7,9,12,14,16,18,	3.0		5.2		
			LEDs off					
6	16	Socket pins source	24 pin/pins 2,4,6,8,10,13,14,16,18,19,	9.5		10.5		
			21,23	9.5		10.5		
			20 pin/pins 2,4,6,8,11,13,15,17,19	9.5		10.5		
	17	Socket pins TTL high	24 pin/pins 1,3,5,7,9,11,15,17,20,22	3.0		5.2		Note[b]
			20 pin/pins 1,3,5,7,9,12,14,16,18	3.0		5.2		

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels, refer to step 12.

Table 4-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	KM	6/15/83

Measurement Chart for TI PAL Adapter
10-715-1006-001

STEP	TEST NO	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 to 12[a]
7	18	Socket pins TTL high	24 pin/pins 2,4,6,8,10,13,14,16,18,19,	3.0		5.2		Note[b]
			21,23	3.0		5.2		
	18		20 pin/pins 2,4,6,8,11,13,15,17,19	3.0		5.2		Note[b]
7	19	Socket pins source	24 pin/pins 1,3,5,7,9,11,15,17,20,22	9.5	--	10.5		Nobe[b]
			20 pin/pins 1,3,5,7,9,12,14,16,18	9.5		10.5		
8	20	Backwards device test	24 pin/pin 24 20 pin/pin 20					CAUTION[a]
								Load with 10 to ground, confirm
								error 32.
9	21	Overcurrent test						CAUTION[a]
		Low range V_{CC}	24 pin/pin 24 20 pin/pin 20					Load with 20 5W to ground,
								confirm error 31.
		Low range CS switch	24 pin/pin 13					Load with 30 5W to ground,
								confirm error 31.
		Low range bit switch 1	24 pin/pin 19					Load with 30 5W to ground,
								confirm error 31.
		Low range bit switch 2	24 pin/pin 14					Load with 30 5W to ground,
								confirm error 31.
								CAUTION[a]

[a]Insert load resistor after pressing START; remove immediately after performing test.
[b]Voltage levels are for calibration purposes only and are not the specified levels of the device manufacturer. For manufacturer-specific levels, refer to step 12.

Table 4-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P.E	DATE
A	Release	KM	6/15/87

Measurement Chart for TI PAL Adapter
10-715-1006-001

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION Socket/pins or circuit board test points	MEASUREMENT MIN	MEASUREMENT NOM	MEASUREMENT MAX	ADJUSTMENT LOCATION	COMMENTS Ground pin 10 or 12[a]
10	22	Overcurrent test						Same loads as step 9, confirm no
		High range	24 pin/pin 24 20 pin/pin 20					errors.[a]
	23	High range V_{CC}	24 pin/pin 24 20 pin/pin 20					Load with 5 5W to ground,
								confirm error 31.
10	23	High range CS switch	24 pin/pin 13					Load with 12 5W to ground,
								confirm error 31.
		High range BIT switch 1	24 pin/pin 19					Load with 12 5W to ground,
								confirm error 31.
		High range BIT switch 2	24 pin/pin 14					Load witn 12 5W to ground,
								confirm error 31.
11	24	Waveform observation	Refer to timing diagram (step					Verify waveforms per timing
		security fuse	11) for test points, family					diagrams.[b]
			pin code, and waveforms.					
12	25	Static programming						Note[b,c]
		Levels V_{CC} Gen V_{IHH}	20 pin/pin 20	10.25		10.75		Voltages are for fuse Ø.
		CE Gen V_{IHH}	20 pin/pin 1	10.25		10.75		
		BIT Gen V_{IHH}	20 pin/pin 19	10.25		10.75		Levels can be measured for any
								fuse by entering its fuse number.
								See manual for instructions.

[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.
[b]A family pin code must be entered or error 30 will be flagged. See the timing diagrams for valid code.
[c]A fuse number must be entered or default to fuse Ø will occur.

Table 4-3. (Continued)

REVISIONS

LTR	DESCRIPTION	P E	DATE
A	Release	[illegible]	6/15/87

Measurement Chart for TI PAL Adapter
10-715-1006-001

STEP	TEST NO.	TEST DESCRIPTION	MEASUREMENT LOCATION	MEASUREMENT			ADJUSTMENT LOCATION	COMMENTS
			Socket/pins or circuit board test points	MIN	NOM	MAX		Ground pin 10 or 12[a]
13	26	Waveform observation	Refer to timing diagram					Note [b,c]
		Verify array	(step 13) for test points,					
			family pinout code, and waveforms					
14	27	Waveform observation	Refer to timing diagram					Note[b,c]
		Program array	(step 14) for test points,					
			family pinout code, and waveforms					
15	28	Waveform observation	No timing diagram supplied; waveforms					Load RAM for desired pattern.[b]
		Program all fuses (opt)	will vary depending on RAM data					
16	29	Rise time adjust						Load with 100 ohm, 2W 5% to GND
		CE switch		9.0	10.0	11.0µS	R1/701-1941	Adjust R1 for TR2 as shown on
		BIT switch 1		3.0		12.0µS	N/A	timing diagram (this step
		BIT switch 2		8.0		12.0µS	N/A	number)
17	30	Supply linearity						Verify waveforms per
		V_{CC} supply	24 pin/pin 24					timing diagram.
		CE supply	24 pin/pin 16					
		BIT supply	24 pin/pin 19					

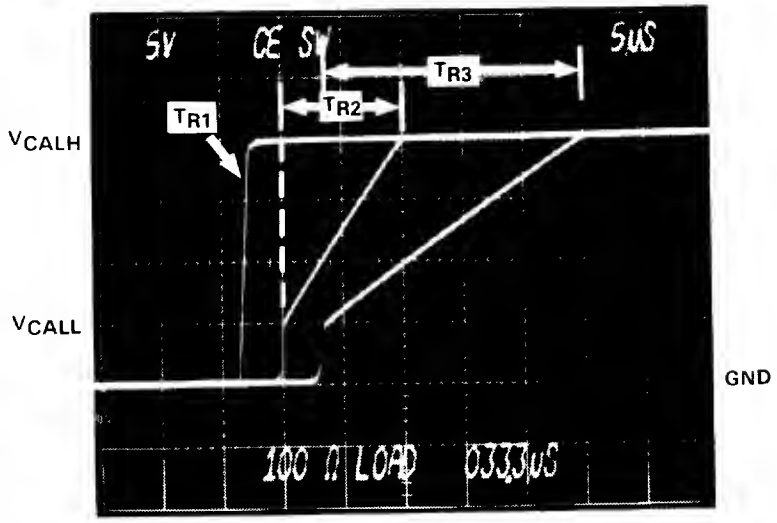
[a]Connect the ground of the DVM to ground pin 10 on a 20-pin socket, to pin 12 on a 24-pin socket, or to pin 14 on a 28-pin socket.

Measurement Chart Photographs

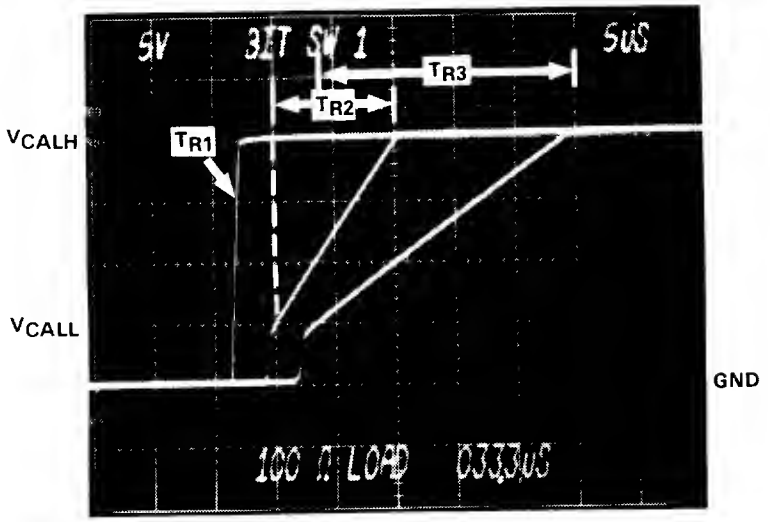
Measurement Chart

PROGRAM ELECTRONICS — RISE TIME WAVEFORM

CHIP ENABLE SWITCH PIN 2

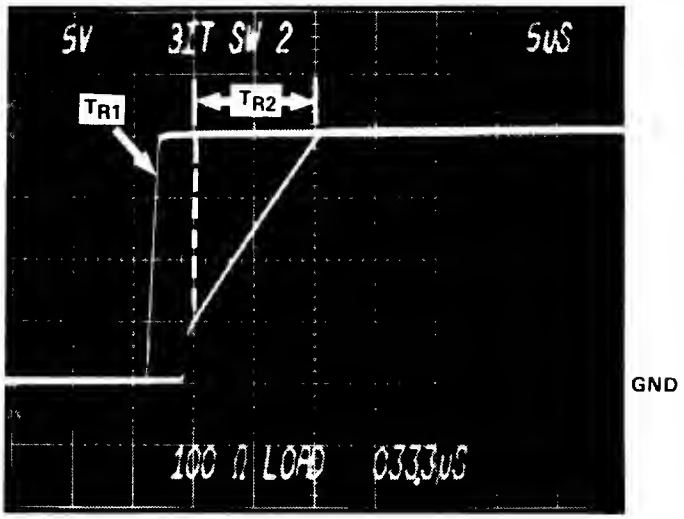


BIT SWITCH 1 PIN 23



DATE	REV	REVISION RECORD	DR	CK

BIT SWITCH 2 PIN 18



	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{CALH}	--	20	--	V	
	V_{CALL}	--	5	--	V	
	T_{R1} CE SW	.450	.650	.850	μs	Adjust R1 on 1941 card for T_{R2} CE SW as shown. Verify that others are within limits. Rise times are measured from V_{CALL} to V_{CALH}. (Voltage levels for reference only).
	T_{R2} CE SW	9.0	10.0	11.0	μs	
	T_{R3} CE SW	15.0	20.0	25.0	μs	
	T_{R1} BIT SW	.450	.650	.850	μs	
	T_{R2} BIT SW	8.0	10.0	12.0	μs	
	T_{R3} BIT SW	15.0	20.0	25.0	μs	

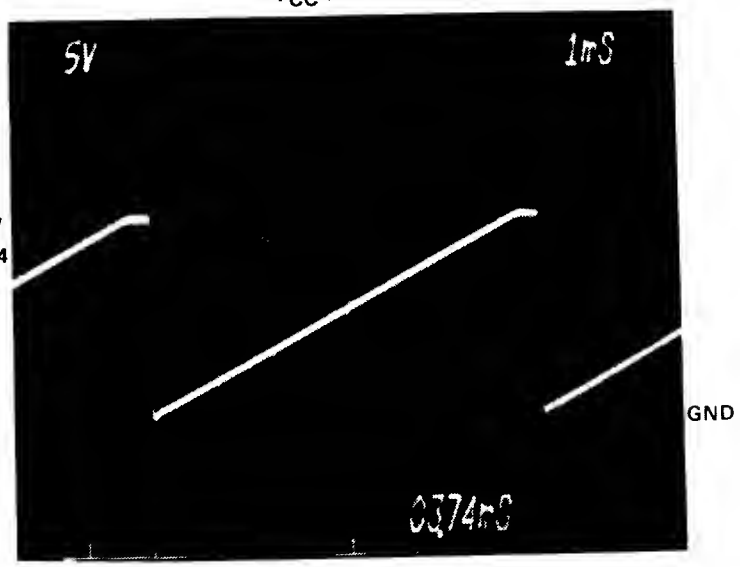
NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Step 16 on the measurement chart.*
3. *Test points are for the 24-pin socket.*
4. *BIT SW rise time limits are for both BIT SW1 and BIT SW2.*
5. *All waveforms shown loaded by 100 Ω 2W 5% resistor to ground.*

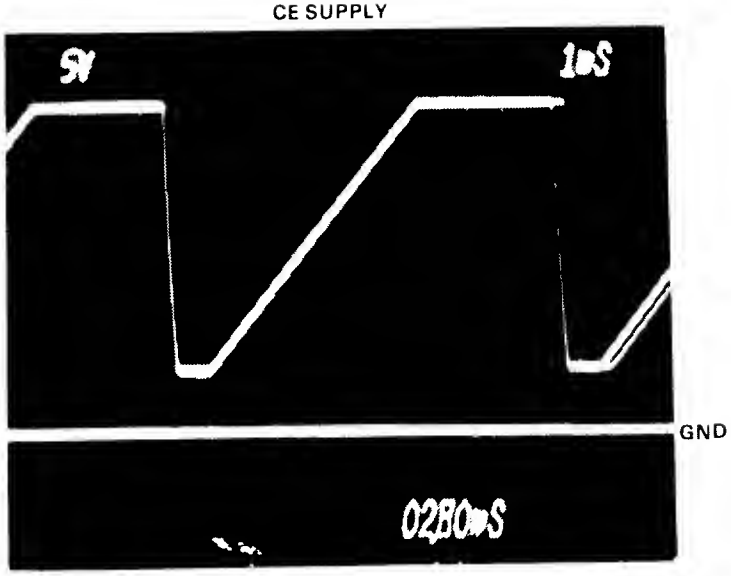
Measurement Chart

PROGRAM ELECTRONICS — SUPPLY LINEARITY

V_{CC} SUPPLY

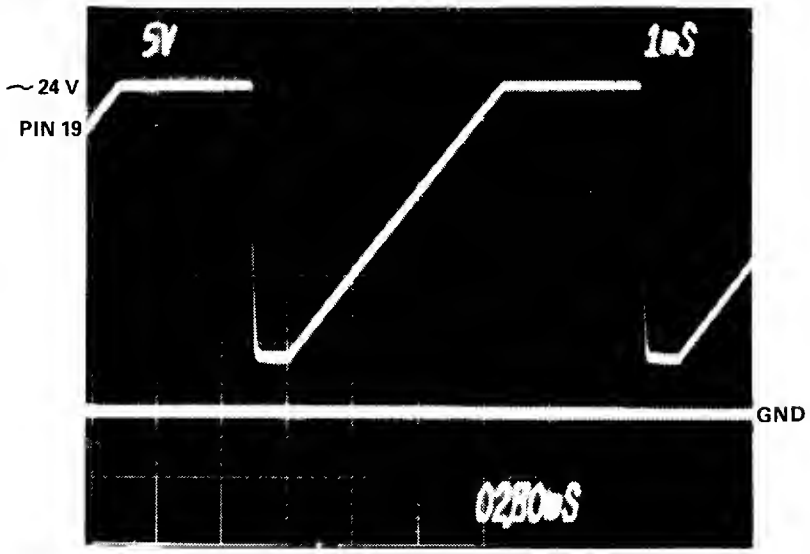


CE SUPPLY



DATE	REV	REVISION RECORD	DR	CK
4/29/93	A	Release	KM	

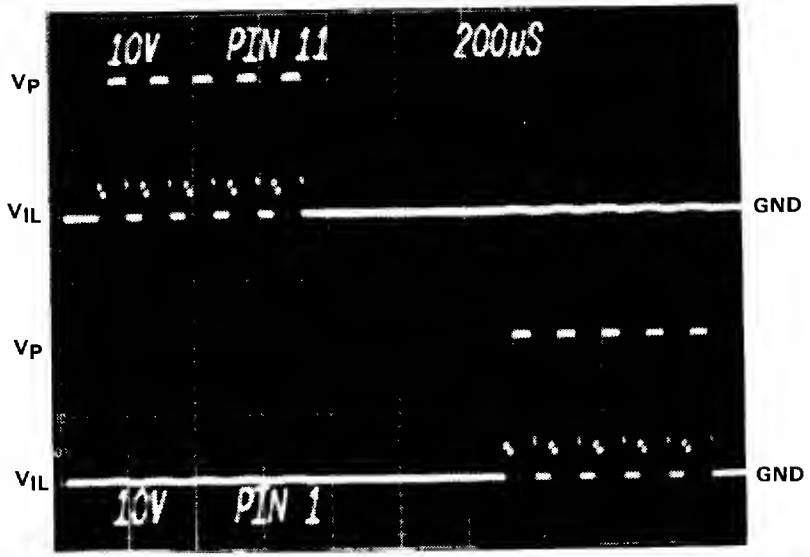
BIT SUPPLY



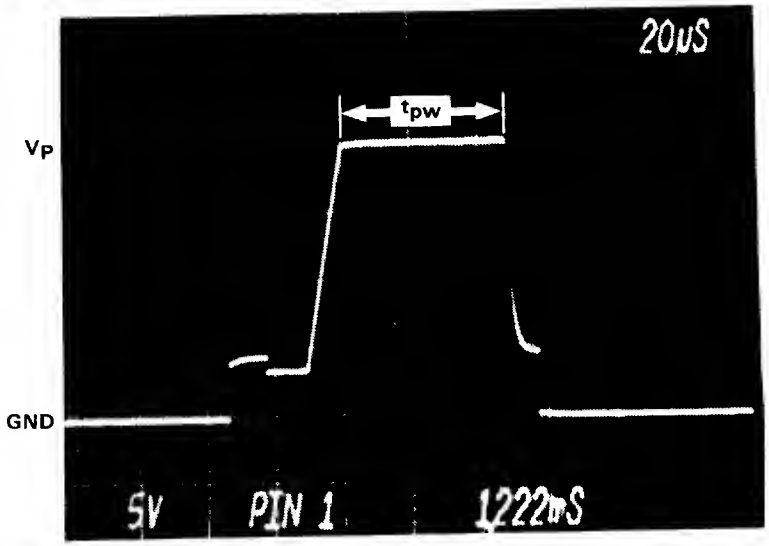
NOTES

1. *Oscilloscope trigger: TP1 1939 card.*
2. *Step 17 on the measurement chart.*
3. *Test points are for the 24-pin socket.*

Timing Diagrams


10V PIN 11 200uS
VP
VIL
GND
VP
VIL
GND
10V PIN 1

1


20uS
tpw
VP
GND
5V PIN 1 1222uS

2

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_P	20.0	21.0	22.0	V	
	V_{IL}			0.8	V	
	t_{pw}	40	50	60	µs	5 Pulses

NOTES

1. *Oscilloscope trigger: t_{p1} 1939 card.*
2. *Cal Step 11 on measurement chart.*
3. *Family pin code 9917.*
4. *Test points are for the 20-pin socket*
5. *Test points are identified on left side of photos.*
6. *Important pulse widths (t_{pw}) and/or rise times (t_r) are identified on photos.*
7. *Oscilloscope horiz. time base setting is identified on top of photos. When delayed sweep is used, the delay time from start of sweep (trigger) is on bottom.*
8. *Oscilloscope vert. voltage settings are identified on photos.*

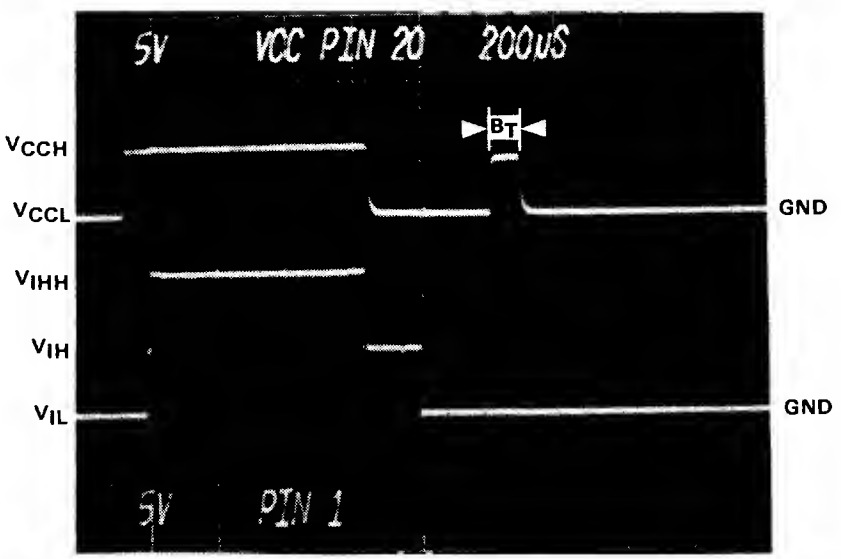
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	6/15/83

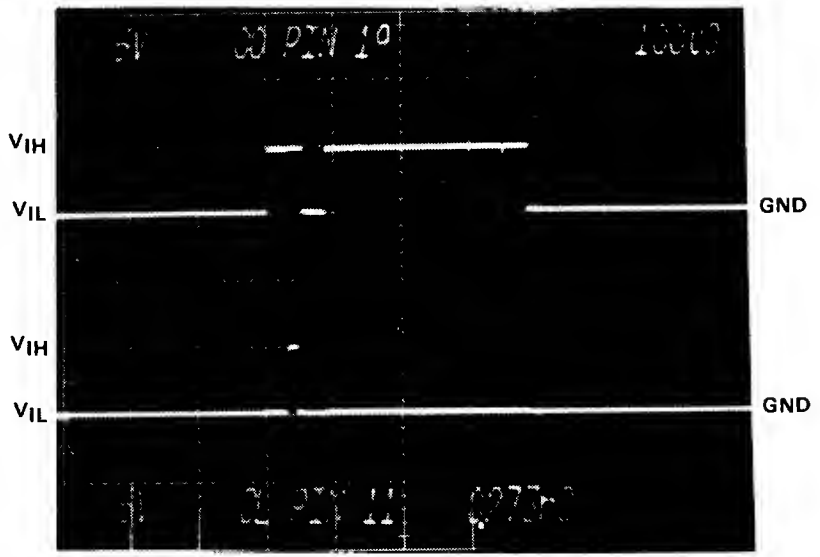
SECURITY FUSE WAVEFORM TIMING DIAGRAM

FAMILY CODE 9917

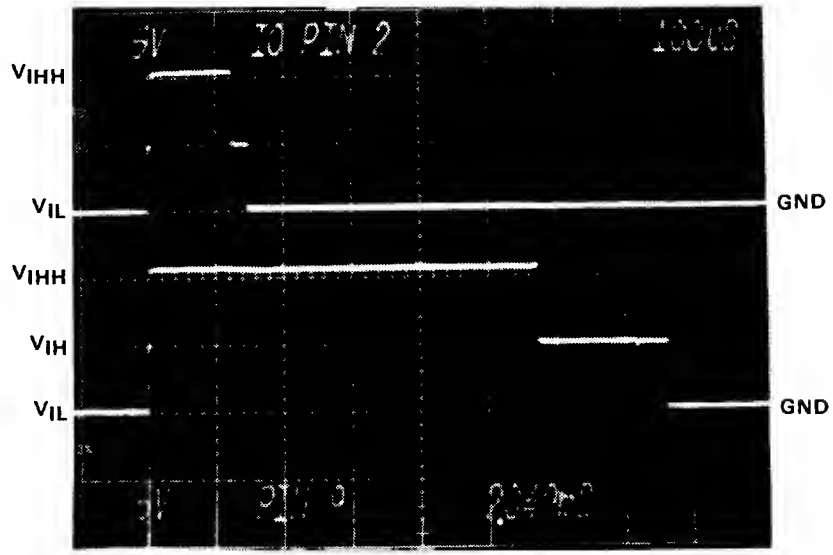
DATA I/O


5V VCC PIN 20 200uS
BT
VCCH
VCCL
VIHH
VIH
VIL
GND
GND
5V PIN 1

1


VIH
VIL
GND
VIH
VIL
GND

2


VIHH
VIL
GND
VIHH
VIH
VIL
GND

3

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IHH}	10.25	10.50	10.75	V	
	V_{IH}	3.0	--	5.2	V	
	V_{IL}		--	0.8	V	
	V_{CCH}	4.75	5.0	5.25	V	
	V_{CCL}	-.4	0	.8	V	
	B_T	--	--	--	--	Backward Device Test
1ST PASS FUSE VERIFY	V_{CC}	4.25	4.50	4.75	V	
2ND PASS FUSE VERIFY	--	5.75	6.00	6.25	V	
1ST PASS FUNCTIONAL VERIFY	V_{CC}	4.65	4.75	4.85	V	
2ND PASS FUNCTIONAL VERIFY	V_{CC}	5.15	5.25	5.35	V	
REJECT COUNT OPTION Ø			5		Pulses	
REJECT COUNT OPTION 1			1		Pulses	

NOTES

1. *Oscilloscope trigger: t_{p1} 1939 card.*
2. *Cal Step 13 on the measurement chart.*
3. *Fuse 32.*
4. *Family pin code 9917.*
5. *Test points are for the 20-pin socket.*
6. *Test points are identified on left side of photos.*
7. *Important pulse widths (t_{pw}) and/or rise times (t_r) are identified on the photos.*
8. *Oscilloscope horiz. time base setting is identified of top of photos. When delayed sweep is used, the delay time from start of sweep (trigger) is on bottom.*
9. *Oscilloscope vert. voltage settings are identified on photos.*

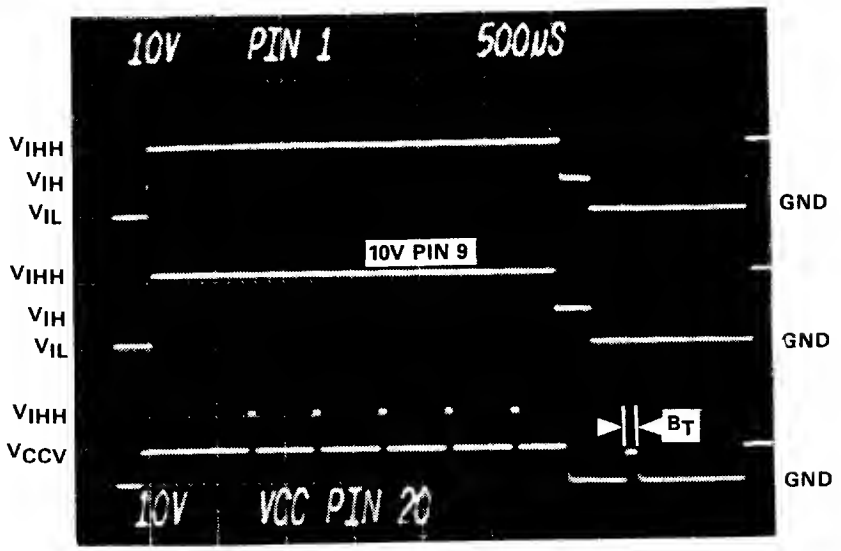
REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	6/14/83

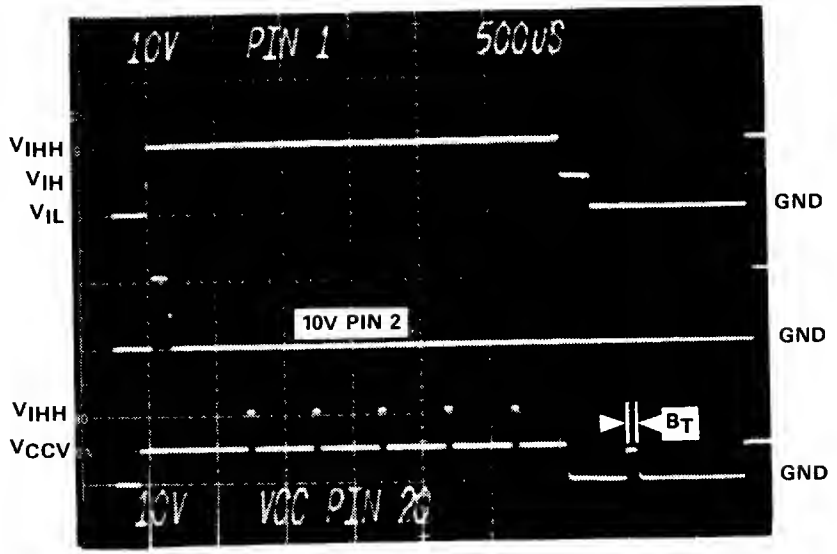
VERIFY WAVEFORM TIMING DIAGRAM

FAMILY CODE 9917

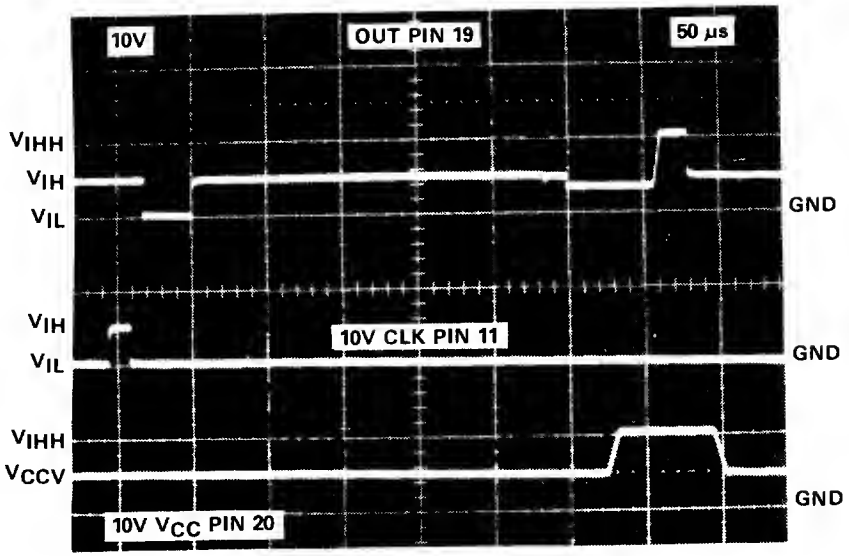
DATA I/O


10V PIN 1 500uS
VIHH
VIH
VIL
GND
10V PIN 9
VIHH
VIH
VIL
GND
VIHH
VCCV
BT
GND
10V VCC PIN 20

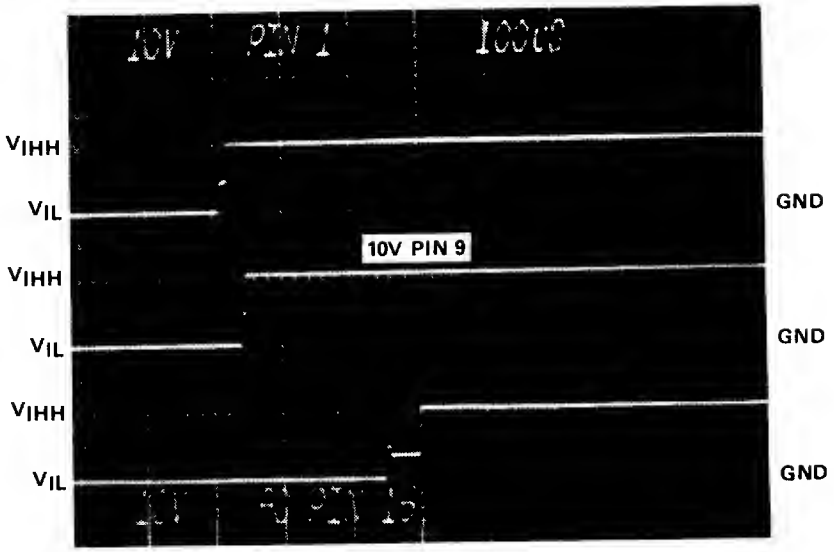
1


10V PIN 1 500uS
VIHH
VIH
VIL
GND
10V PIN 2
GND
VIHH
VCCV
BT
GND
10V VCC PIN 20

2


10V
OUT PIN 19
50 µs
VIHH
VIH
VIL
GND
VIH
VIL
10V CLK PIN 11
GND
VIHH
VCCV
GND
10V VCC PIN 20

3


VIHH
VIL
GND
10V PIN 9
VIHH
VIL
GND
VIHH
VIL
GND

4

FAMILY CHARACTERISTICS

	VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
PROGRAM	V_{IHH}	10.25	10.50	10.75	V	
	V_{CCV}	4.8	--	5.2	V	
	V_{IH}	3.0	--	5.2	V	
	V_{IL}			0.8	V	
	t_{pw1}	10.0		50.0	us	
	t_{pw2}	1.0			us	
	t_{pw3}	1.0			us	
	B_T	--	--	--	--	Backward Device Test
1ST PASS FUSE VERIFY	V_{CC}	4.25	4.50	4.75	V	
2ND PASS FUSE VERIFY	--	5.75	6.00	6.25	V	
1ST PASS FUNCTIONAL VERIFY	V_{CC}	4.65	4.75	4.85	V	
2ND PASS FUNCTIONAL VERIFY	V_{CC}	5.15	5.25	5.35	V	
REJECT COUNT OPTION Ø			5		Pulses	
REJECT COUNT OPTION 1			1		Pulses	

NOTES

1. *Oscilloscope trigger: t_{p1} 1939 card.*
2. *Cal Step 14 on the measurement chart.*
3. *Fuse 32.*
4. *Family pin code 9917.*
5. *Test points are for the 20-pin socket.*

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	6/15/83

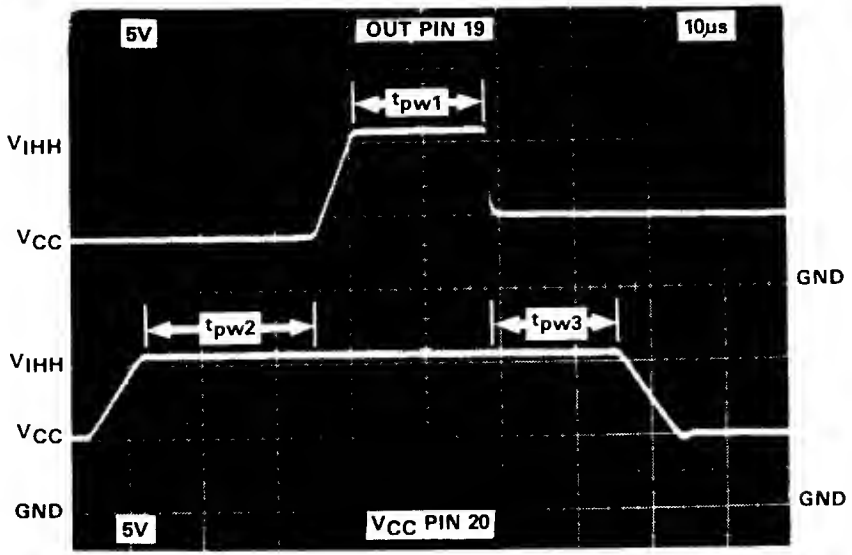
PROGRAMMING WAVEFORM TIMING DIAGRAM

FAMILY CODE 9917

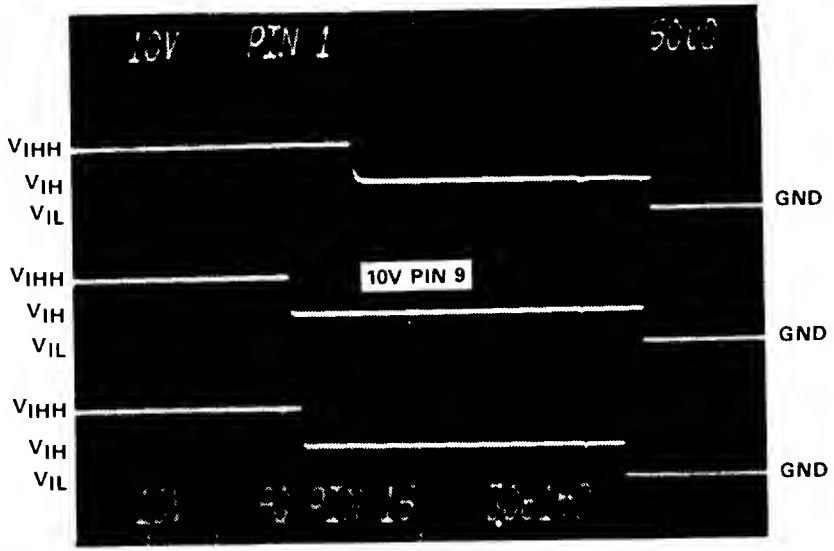
SHEET 1 OF 2

DATA I/O

0526 1282


5V
OUT PIN 19
10µs
tpw1
VIHH
VCC
GND
tpw2
tpw3
VIHH
VCC
GND
5V
VCC PIN 20
GND

5


10V PIN 1
VIHH
VIH
VIL
GND
10V PIN 9
VIHH
VIH
VIL
GND
VIHH
VIH
VIL
GND

6

REVISIONS

LTR	DESCRIPTION	P.E.	DATE
A	Release	KM	6/14/83

PROGRAMMING WAVEFORM TIMING DIAGRAM

FAMILY CODE 9917

SHEET 2 OF 2

DATA I/O

SECTION 5

CIRCUIT DESCRIPTION

5.1 INTRODUCTION

This section defines the functions of the LogicPak™ P/T adapters' principal components. The circuit board assembly is depicted by a block diagram accompanied by a written description.

5.2 GENERAL ARCHITECTURE

The adapters interface with the LogicPak™. When they are installed, they customize the PLDS to support a specific family of logic devices.

5.3 COMPONENT LAYOUT

A typical block diagram is shown in figure 5-1, and the schematic is at the back of this manual. The adapter board routes all the necessary signals required to perform fuse operations and functional tests of the logic devices. These signals are routed to two sockets to support the pin counts of the devices. The socket enabled by the family pinout code is identified by the lighting of the appropriate socket LED.

Programming voltage levels are routed to a clamping R-C network, which is precharged to the programming voltage potentials. When the programming pulses are presented to the device pins, the network prevents overshoot.

A backward test circuit connects to the V_{CC} pin of each socket. The circuitry tests the orientation of the logic device in its socket. If it is incorrect, an error code will be flagged and operation will stop. The test method limits power to the device, thereby preventing damage to it.

Firmware specific to the device manufacturer's family of logic is resident in an EPROM, which receives its address and select inputs from the LogicPak™. The PROM outputs are buffered by an octal data gate, whose inputs feedback to the data base within the LogicPak™. Fuse programming, verification, and functional testing algorithms are stored in PROM and are referenced by stored family and device pinout codes.

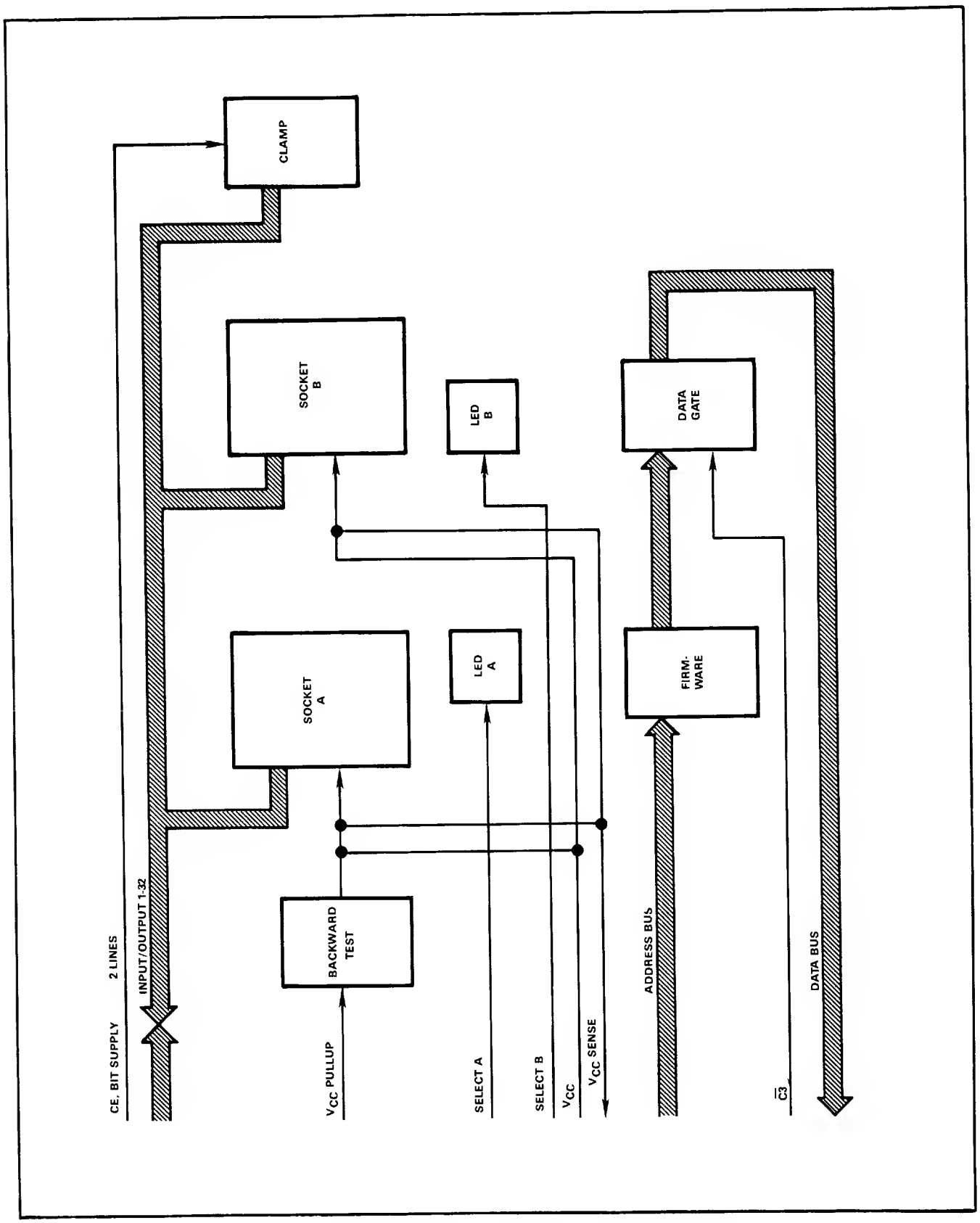


Figure 5-1. Typical Programming/Testing Adapter Block Diagram

APPENDIX A

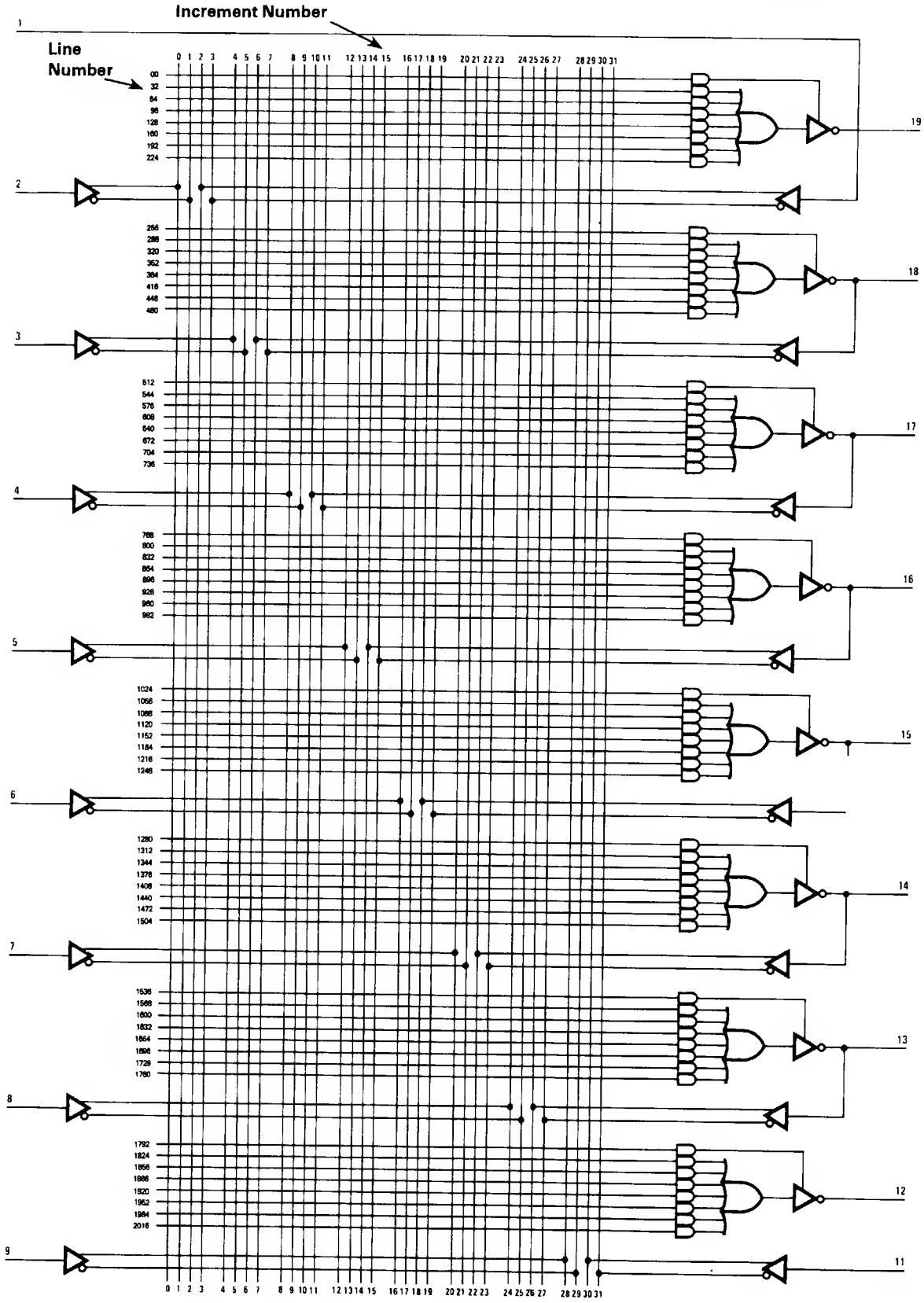
FUNCTIONAL DIAGRAMS
FAMILY AND PINOUT CODES

Table A-1. TI PAL Device Support List

Device	Family/ Pinout Code	LogicPak™ Version No.	P/T Adapter 303A-006 Version No.	Design Adapter 303A-100 Version No.
PAL 16L8A	99/17	V01	V03	V01
PAL 16R4A	99/24	V01	V03	V01
PAL 16R6A	99/24	V01	V03	V01
PAL 16R8A	99/24	V01	V03	V01
TIBPAL16L8	99/17	V01	V03	V01
TIBPAL16R4	99/24	V01	V03	V01
TIBPAL16R6	99/24	V01	V03	V01
TIBPAL16R8	99/24	V01	V03	V01
PAL 20L8A	99/26	V01	V03	V01
PAL 20R4A	99/27	V01 +	V03	V01
PAL20R6A	99/27	V01 +	V03	V01
PAL20R8A	99/27	V01 +	V03	V01
TIBPALR19L8	99/89	V01	V03	
TIBPALR19R4	99/91	V01 +	V03	
TIBPALR19R6	99/91	V01 +	V03	
TIBPALR19R8	99/91	V01 +	V03	
TIBPALT19L8	99/88	V01	V03	
TIBPALT19R4	99/90	V01 +	V03	
TIBPALT19R6	99/90	V01 +	V03	
TIBPALT19R8	99/90	V01 +	V03	

+ LogicPak Version V04 required for full support of device register preload feature.

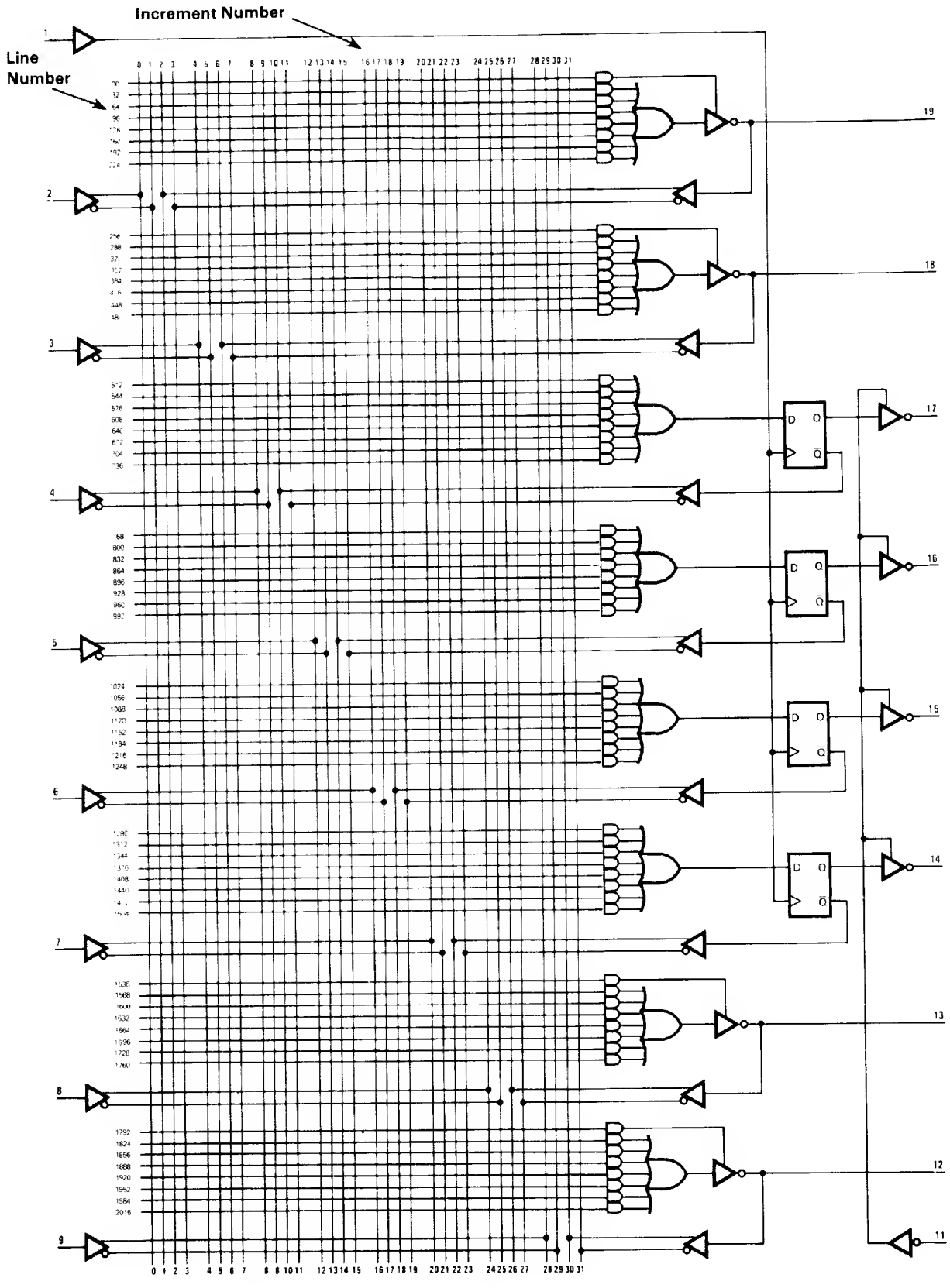
Logic Diagram PAL16L8A, TIBPAL16L8



NOTE: Fuse number = Increment Number + Line Number

Figure A-1. Logic Diagram PAL16L8A, TIBPAL16L8

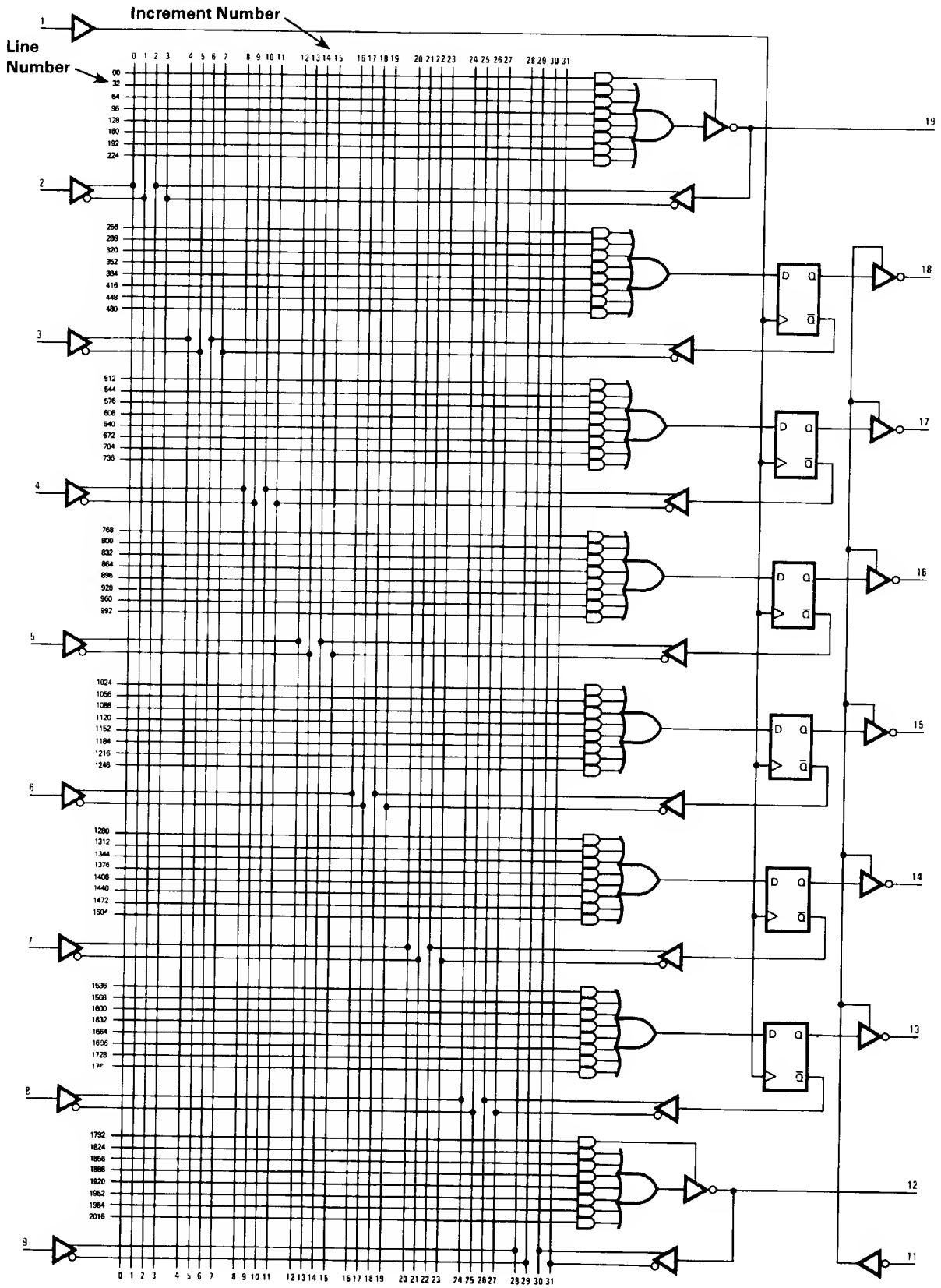
Logic Diagram PAL16R4A, TIBPAL16R4



NOTE: Fuse number = Increment Number + Line Number

Figure A-2. Logic Diagram PAL16R4A, TIBPAL16R4

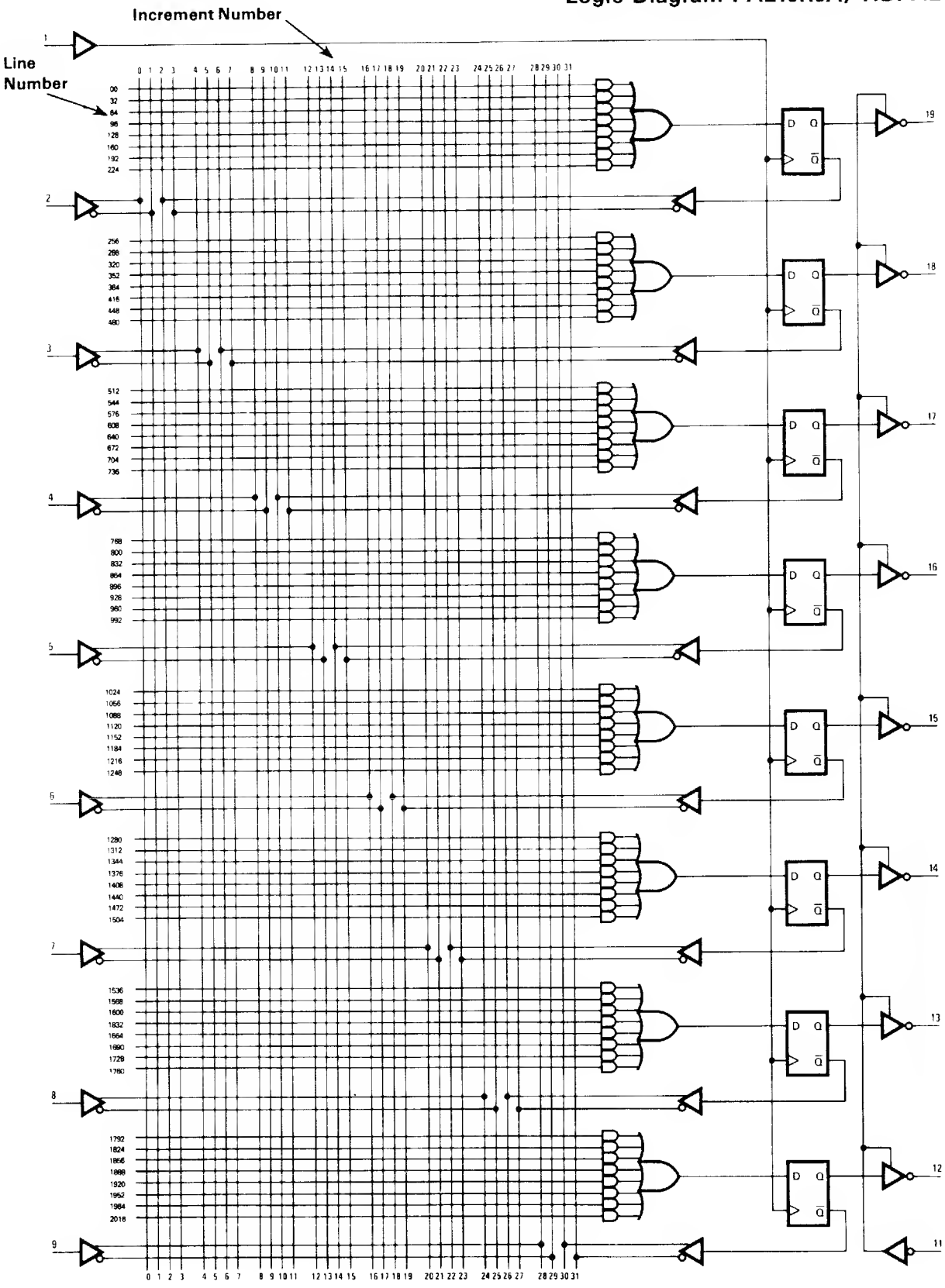
Logic Diagram PAL16R6A, TIBPAL16R6



NOTE: Fuse number = Increment Number + Line Number

Figure A-3. Logic Diagram PAL16R6A, TIBPAL16R6

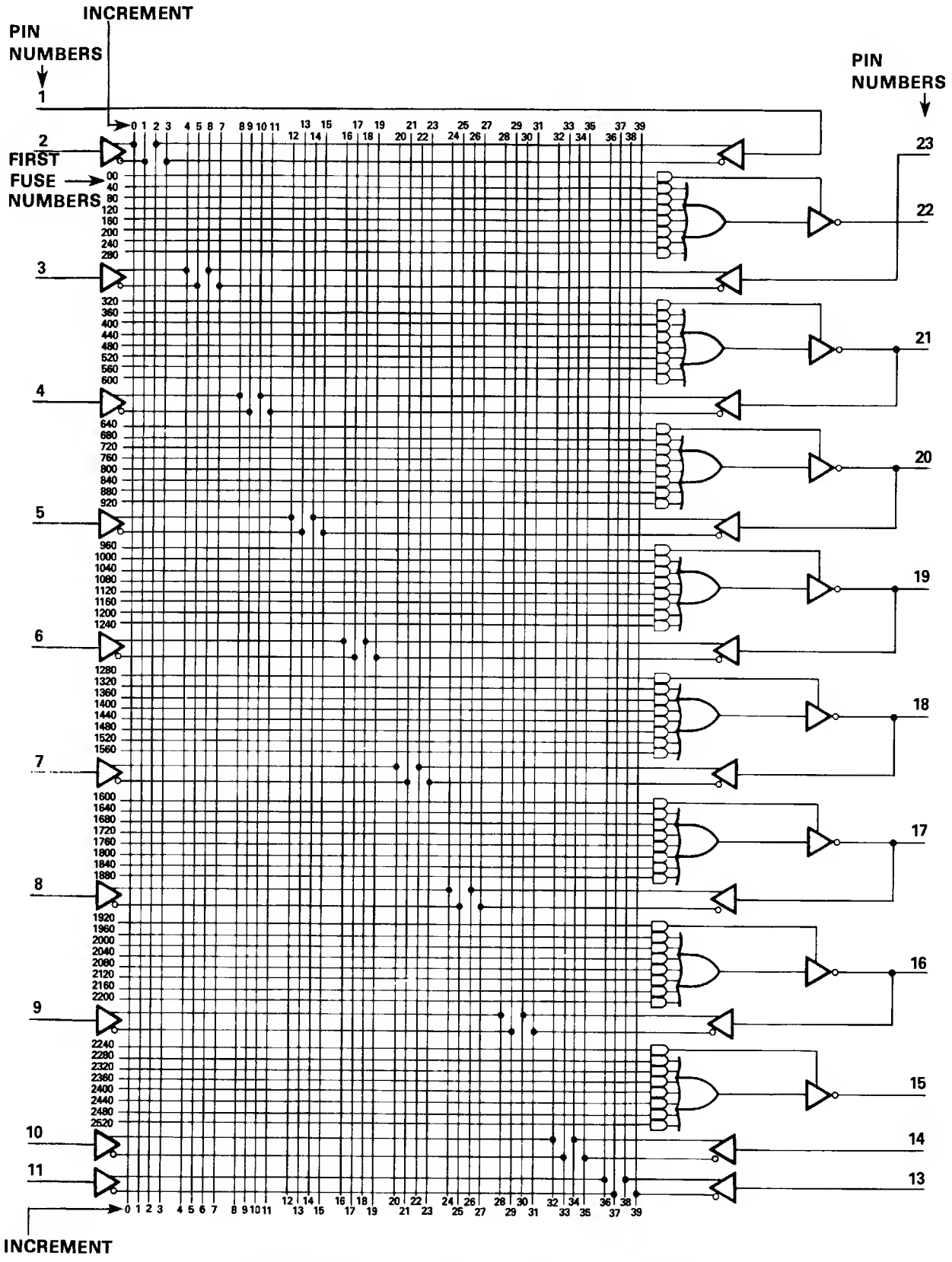
Logic Diagram PAL16R8A, TIBPAL16R8



NOTE: Fuse number = Increment Number + Line Number

Figure A-4. Logic Diagram PAL16R8A, TIBPAL16R8

Logic Diagram PAL20L8A



NOTE: Fuse Number = First Fuse Number + Increment

Figure A-5. Logic Diagram PAL20L8A

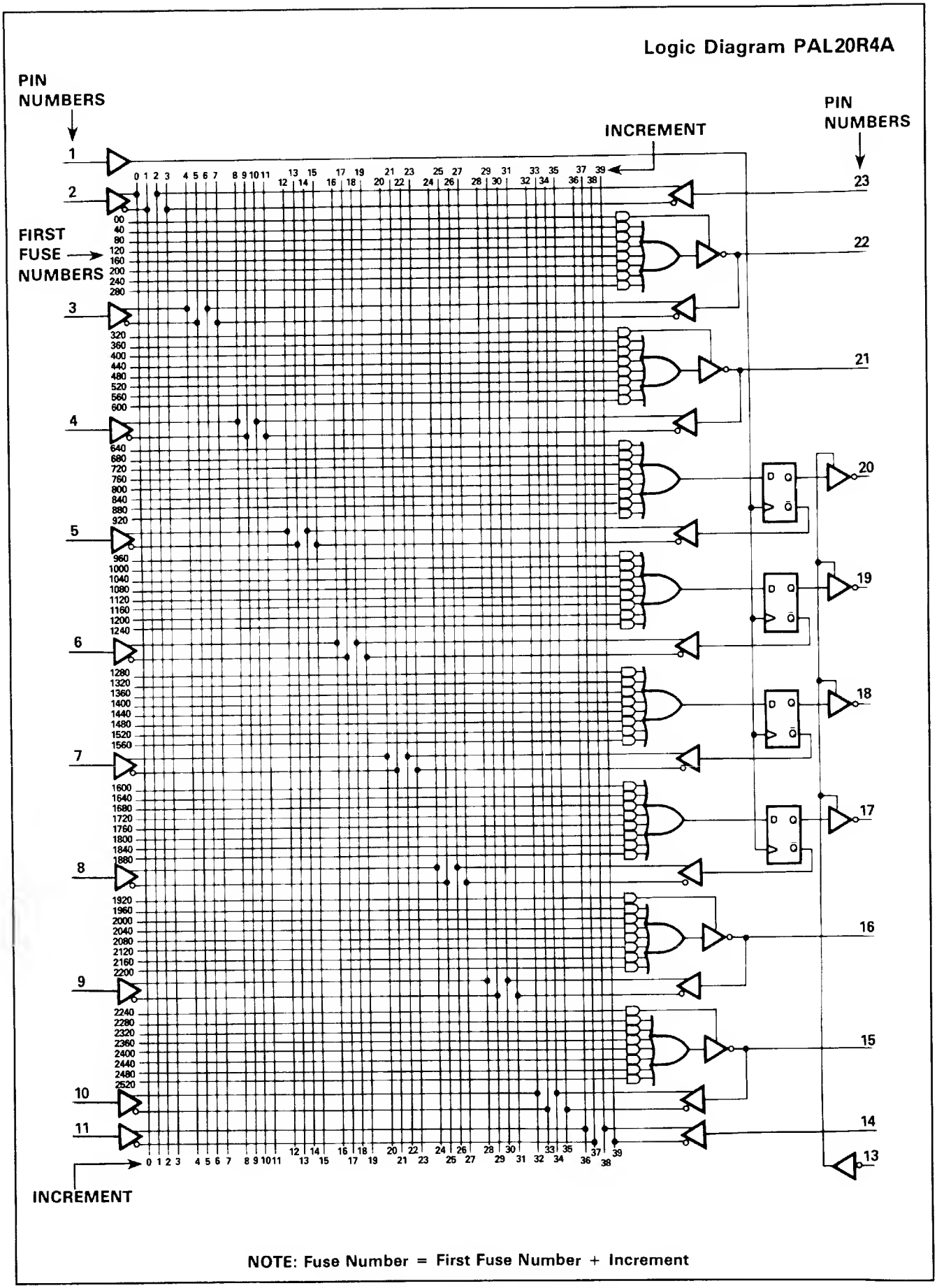


Figure A-6. Logic Diagram PAL20R4A

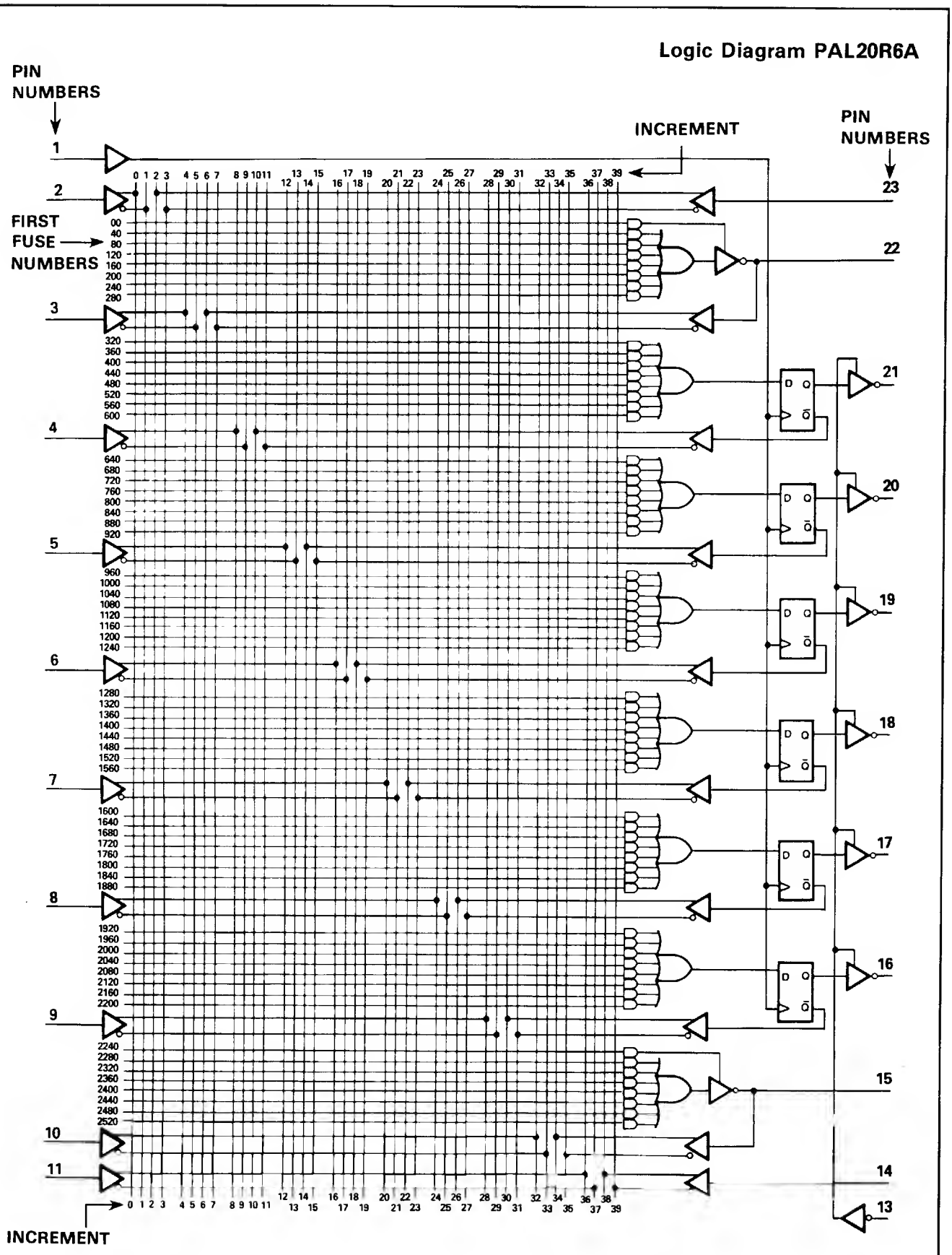


Figure A-7. Logic Diagram PAL20R6A

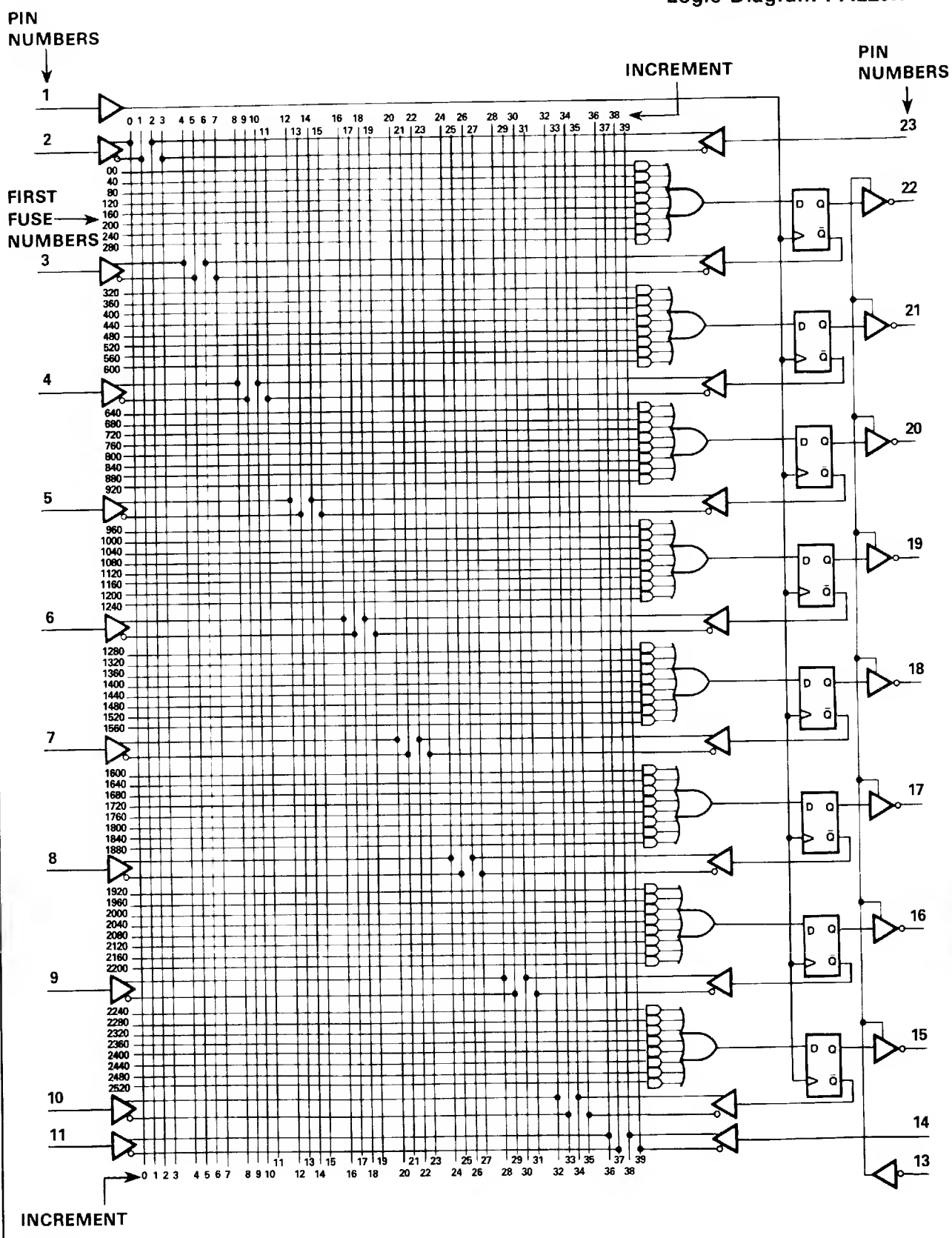


Figure A-8. Logic Diagram PAL20R8A

Logic Diagram TIBPALR19L8

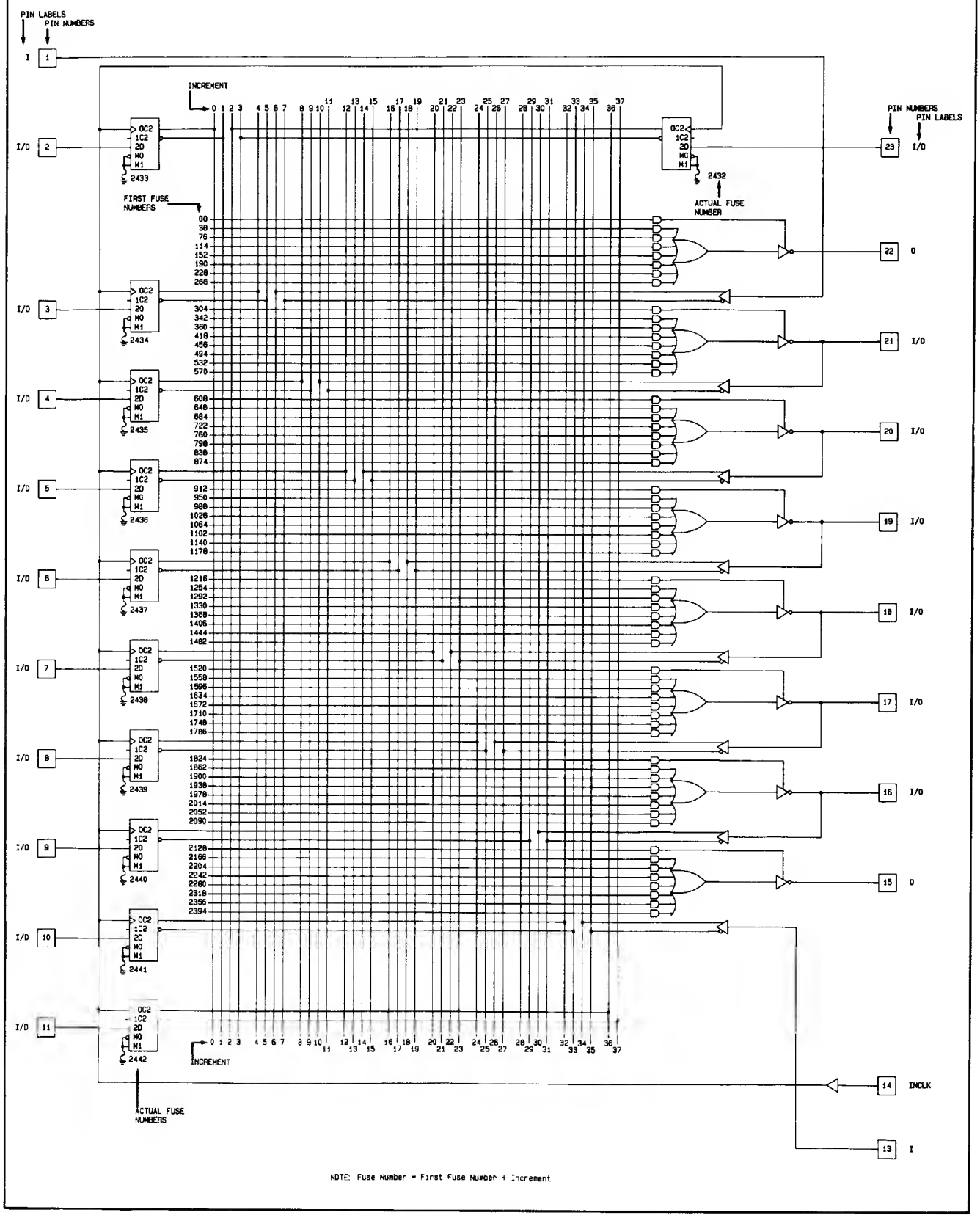


Figure A-9. Logic Diagram TIBPALR19L8

Logic Diagram TIBPALR19R4

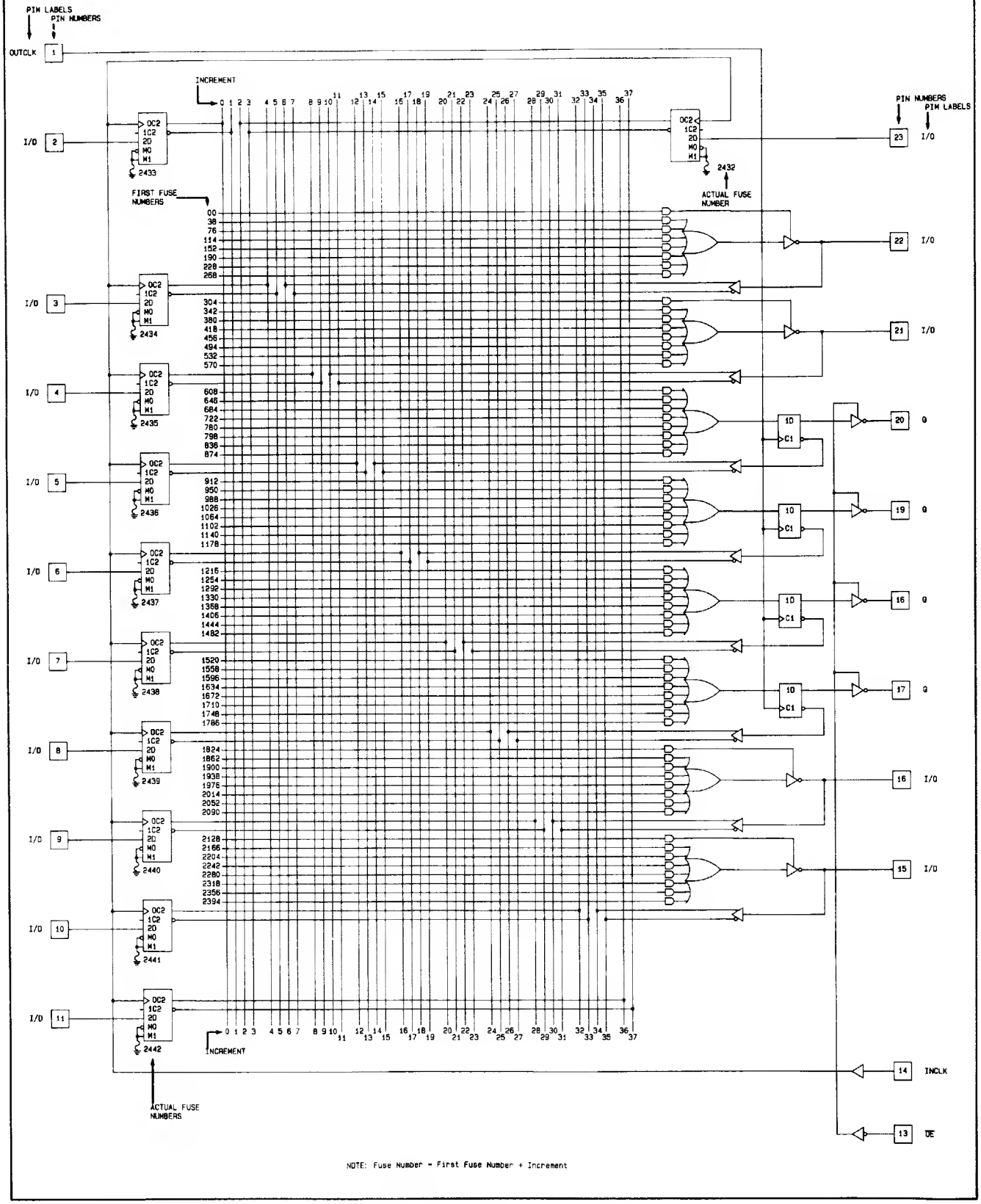


Figure A-10. Logic Diagram TIBPALR19R4

Logic Diagram TIBPALR19R6

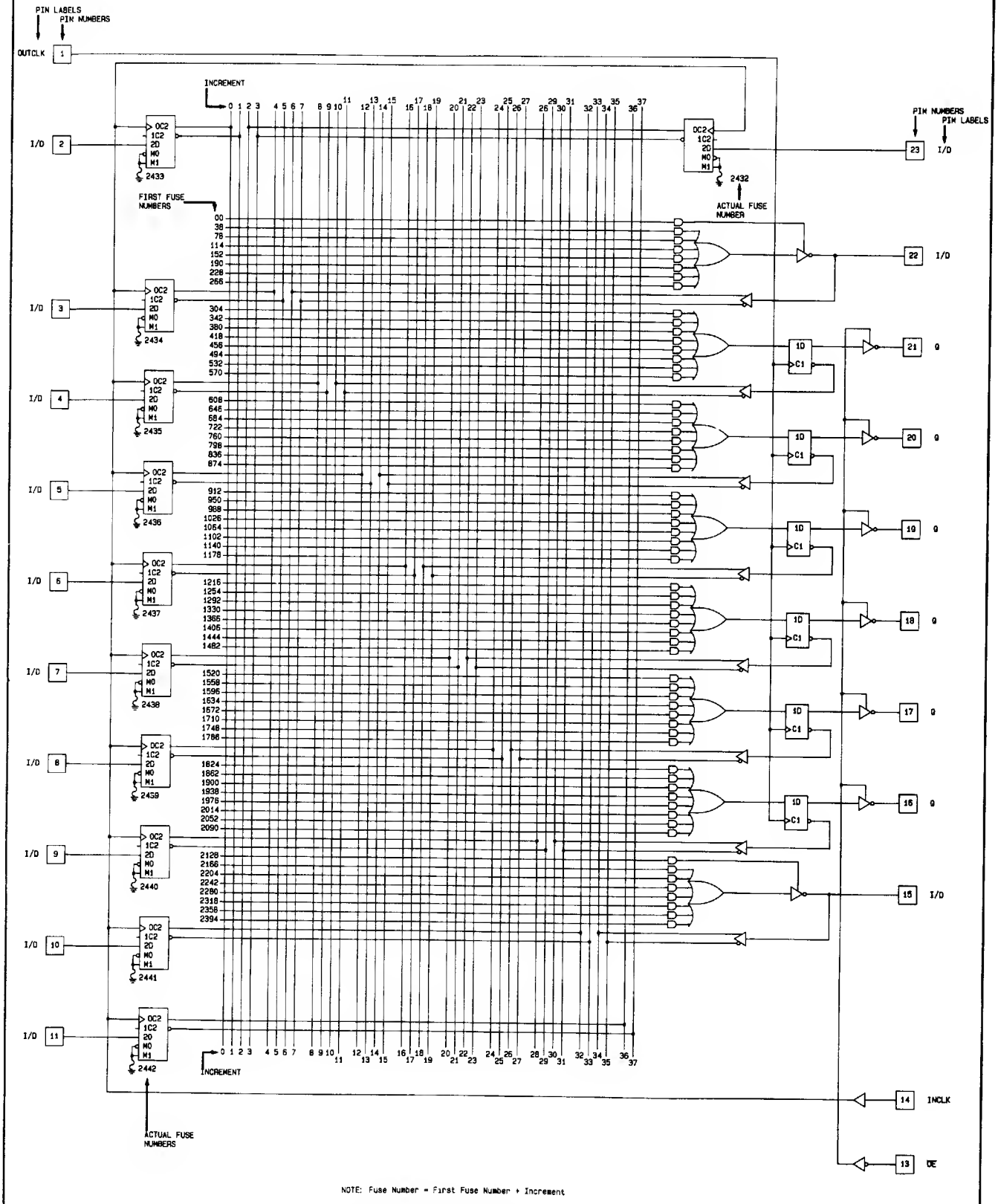


Figure A-11. Logic Diagram TIBPALR19R6

Logic Diagram TIBPALR19R8

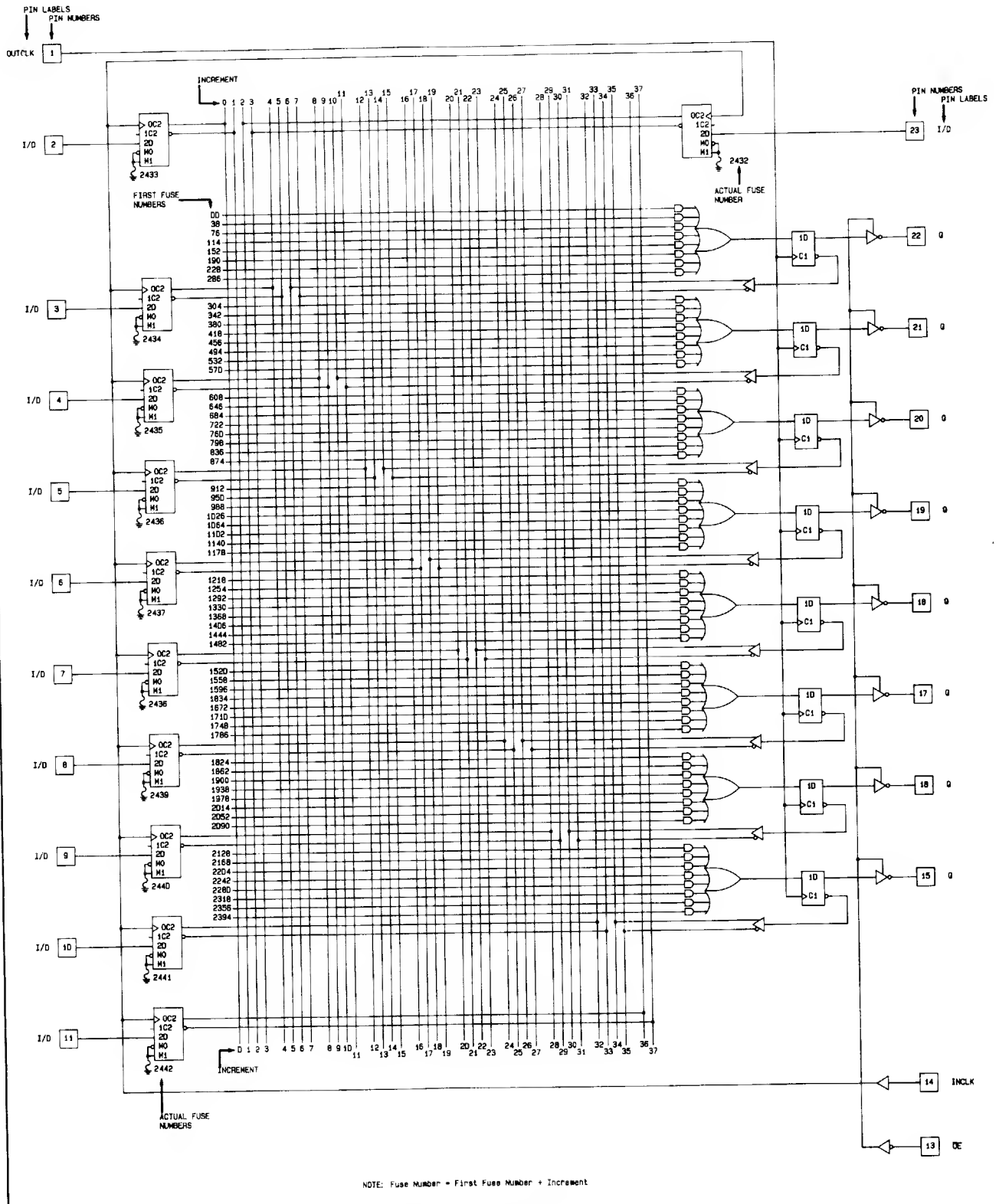


Figure A-12. Logic Diagram TIBPALR19R8

Logic Diagram TIBPALT19L8

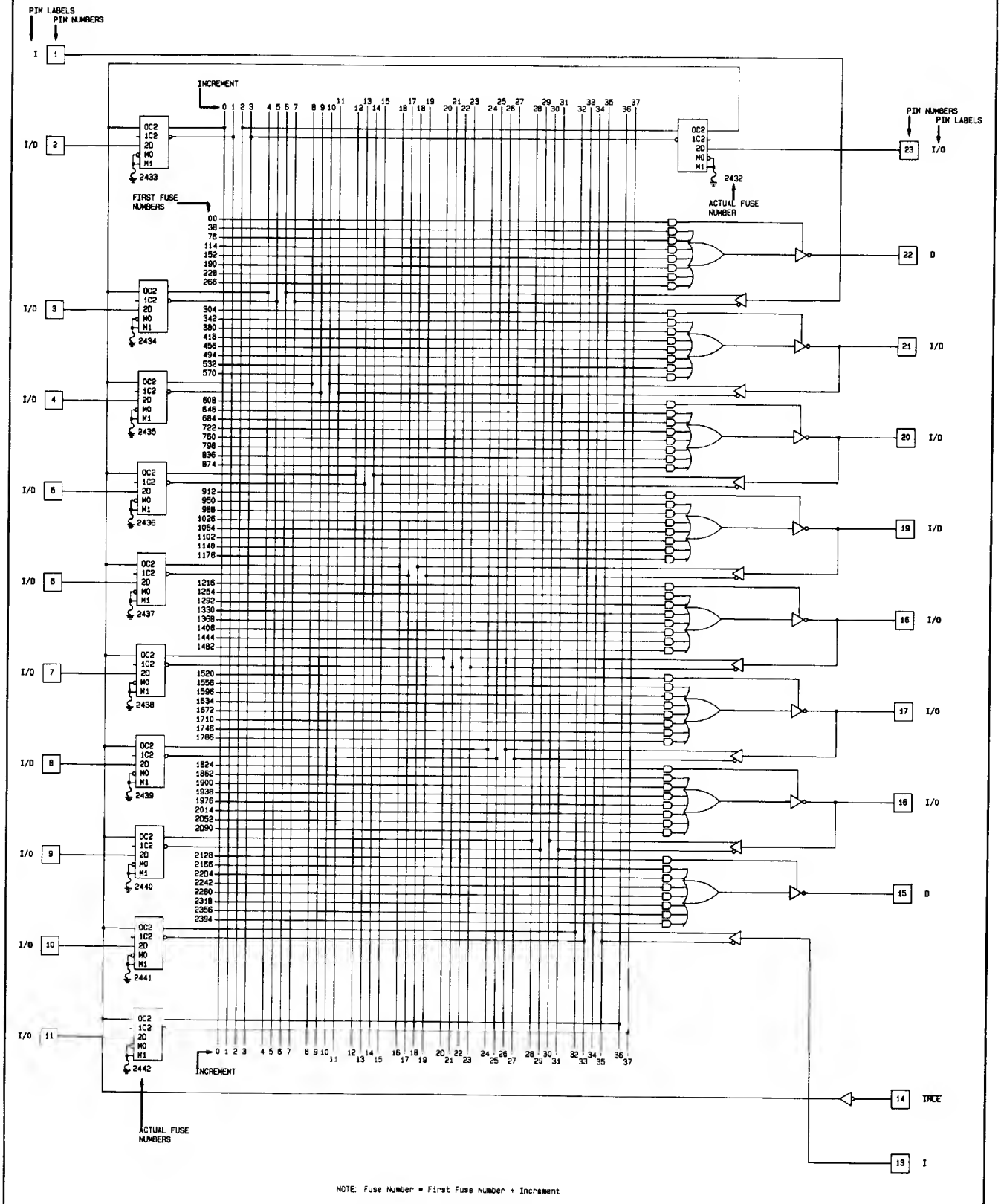


Figure A-13. Logic Diagram TIBPALT19L8

Logic Diagram TIBPALT19R4

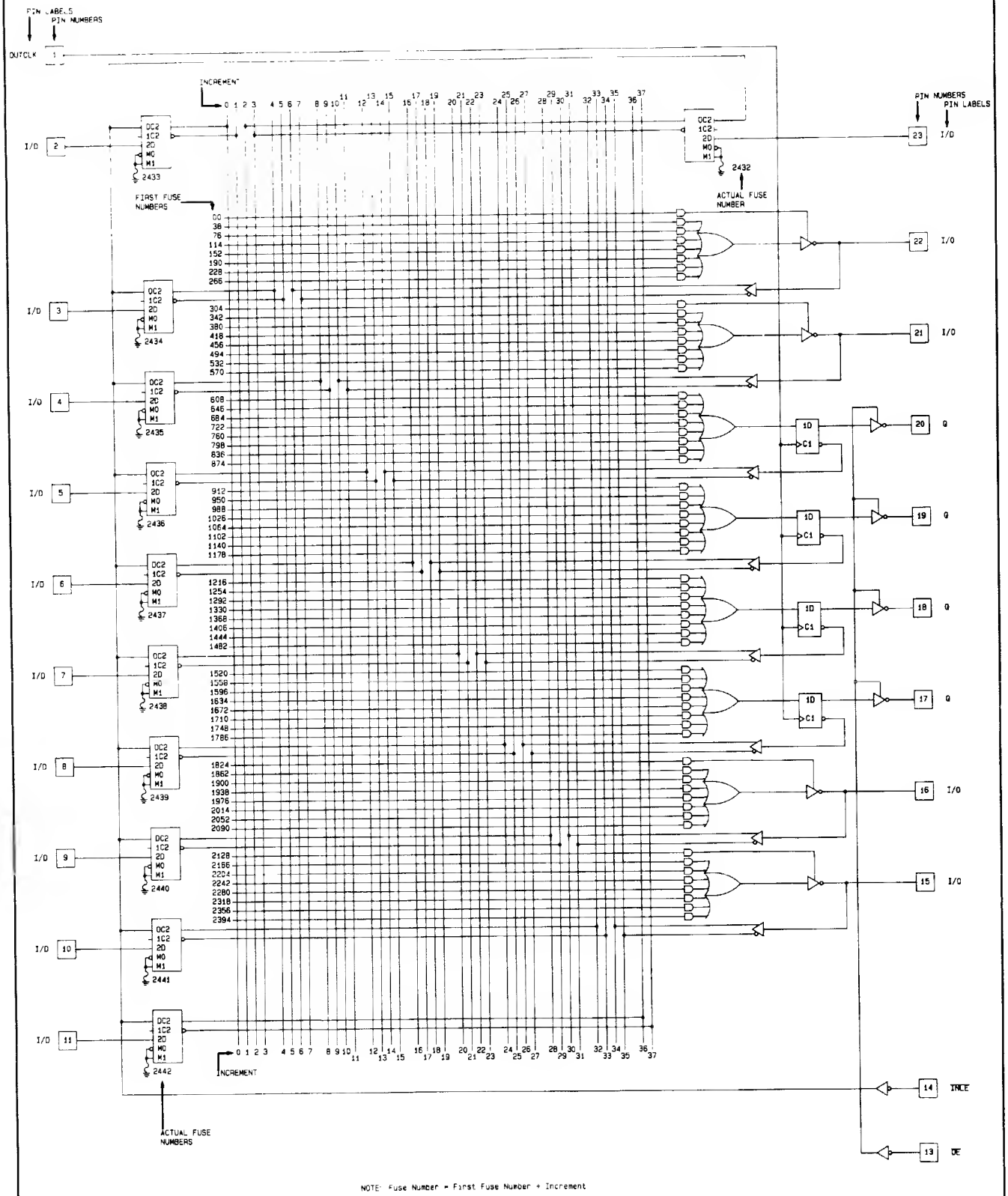


Figure A-14. Logic Diagram TIBPALT19R4

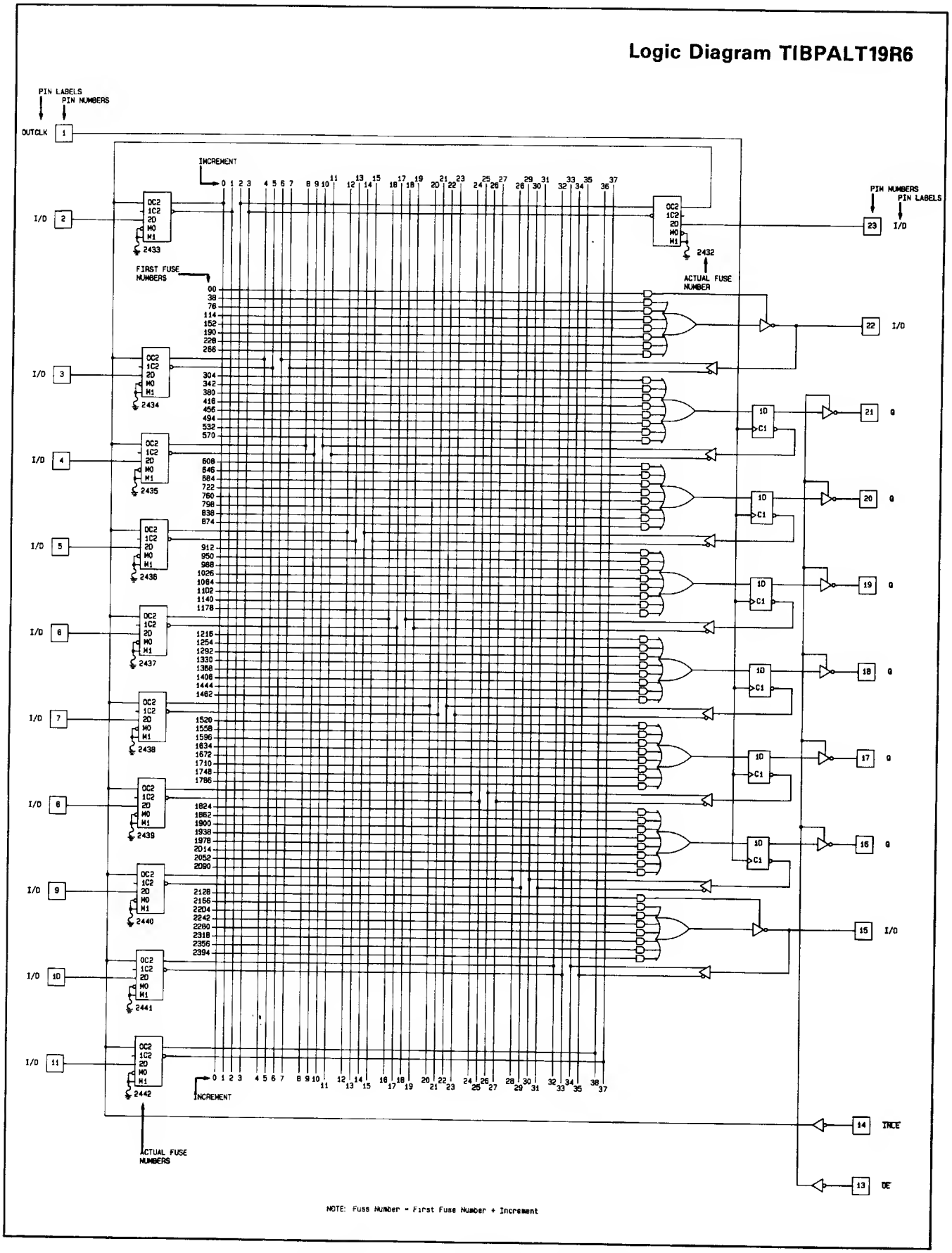


Figure A-15. Logic Diagram TIBPALT19R6

Logic Diagram TIBPALT19R8

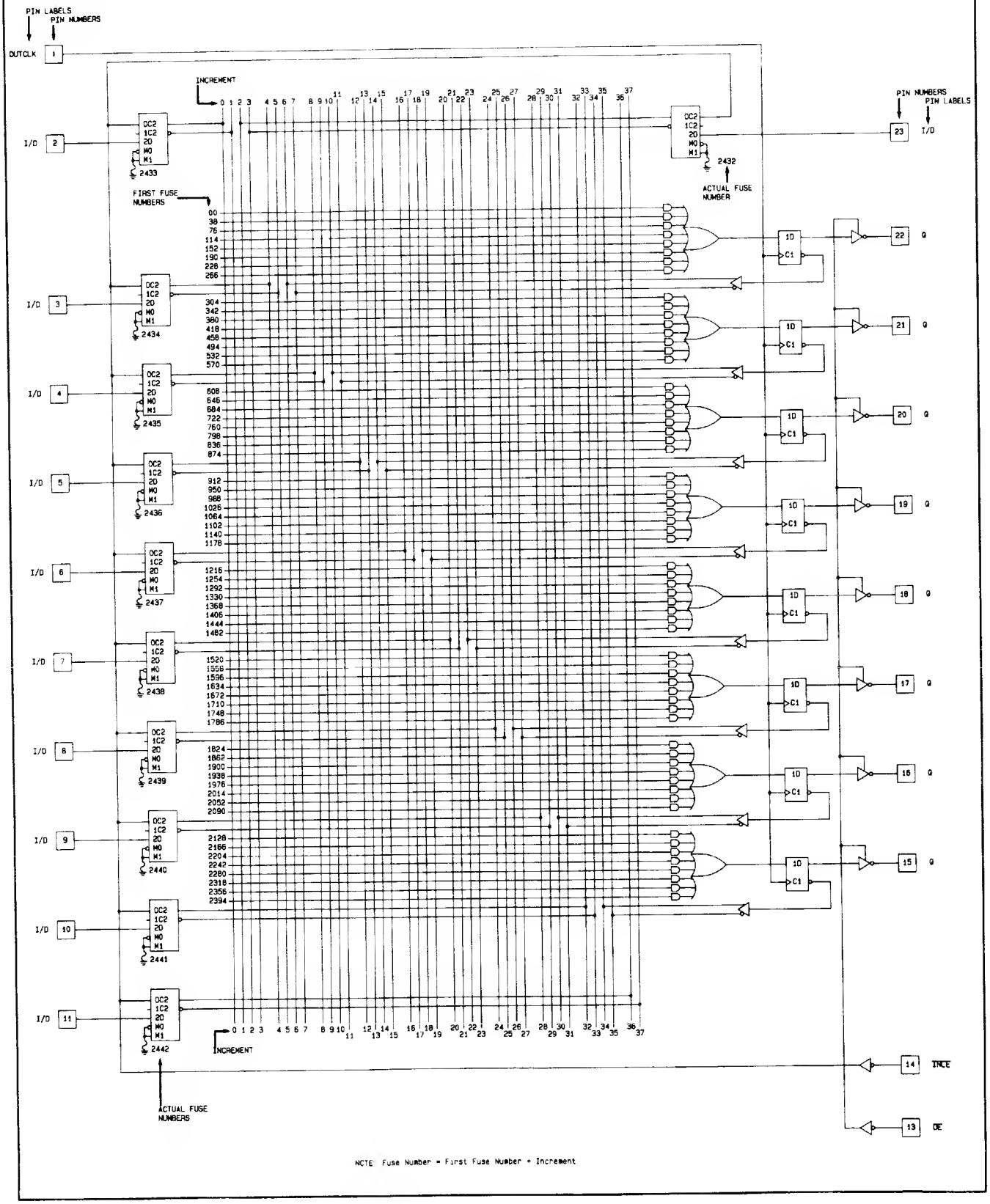
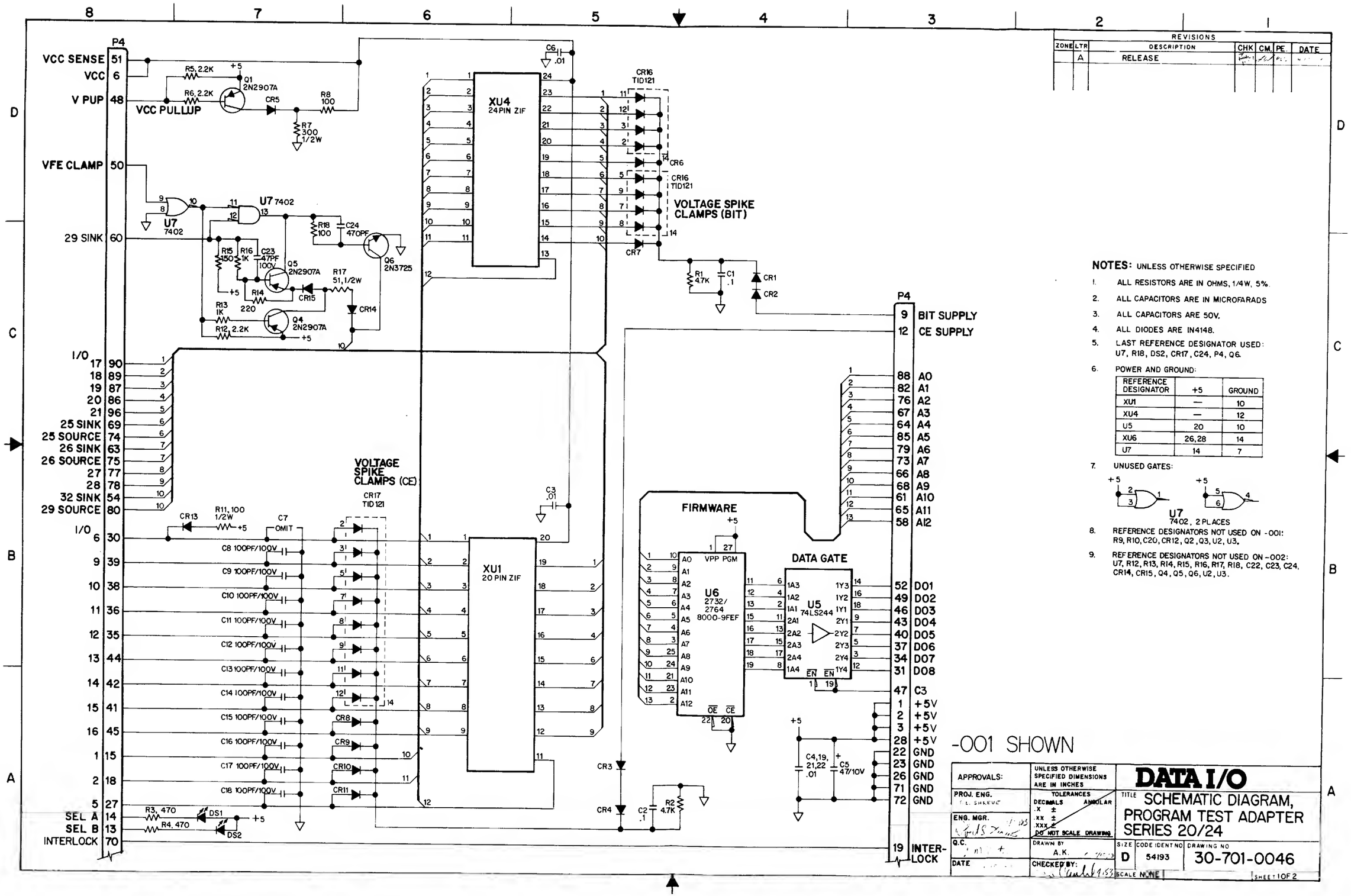


Figure A-16. Logic Diagram TIBPALT19R8

APPENDIX B
SCHEMATIC

30-701-0046 Programming/Testing Adapter



REVISIONS						
ZONE	LTR	DESCRIPTION	CHK	CM.	PE.	DATE
	A	RELEASE				

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS
3. ALL CAPACITORS ARE 50V.
4. ALL DIODES ARE IN4148.
5. LAST REFERENCE DESIGNATOR USED: U7, R18, DS2, CR17, C24, P4, Q6.
6. POWER AND GROUND:

REFERENCE DESIGNATOR	+5	GROUND
XU1	—	10
XU4	—	12
U5	20	10
XU6	26,28	14
U7	14	7

7. UNUSED GATES:

8. REFERENCE DESIGNATORS NOT USED ON -001: R9, R10, C20, CR12, Q2, Q3, U2, U3.
9. REFERENCE DESIGNATORS NOT USED ON -002: U7, R12, R13, R14, R15, R16, R17, R18, C22, C23, C24, CR14, CR15, Q4, Q5, Q6, U2, U3.

-001 SHOWN

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ. ENG. T.L. SHREVE	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM, PROGRAM TEST ADAPTER SERIES 20/24	
ENG. MGR.			
Q.C.	DRAWN BY A.K.	SIZE D	CODE IDENT NO 54193
DATE	CHECKED BY:	SCALE NONE	DRAWING NO 30-701-0046
			SHEET 1 OF 2

REVISIONS						
ZONE	LTR	DESCRIPTION	CHK	CM.	PE	DATE
	A	RELEASE				

P4
VCC SENSE 51
VCC 6
V PUP 48
BIT SW 1 91
VFE CLAMP 50
VCC PULLUP
R5, 2.2K
R6, 2.2K
Q1 2N2907A
CR5
R8 100
R7 300 1/2W
R10 1K
C20 330PF 100V
Q2 2N2484
R9 100
Q3 MJE251
CR12 5FT05 50V
C6 .01
XU4 24PIN ZIF
CR16 TID121
CR6
CR16 TID121
VOLTAGE SPIKE CLAMPS (BIT)
CR7
R1 4.7K
C1 .1
CR1
CR2
P4
9 BIT SUPPLY
12 CE SUPPLY
I/O 17 90
18 89
19 87
20 86
21 96
25 SINK 69
25 SOURCE 74
26 SINK 63
26 SOURCE 75
27 77
28 78
32 SINK 54
29 SOURCE 80
VOLTAGE SPIKE CLAMPS (CE)
CR17 TID121
CR13
R11, 100 1/2W
C7 OMIT
C8 100PF/100V
C9 100PF/100V
C10 100PF/100V
C11 100PF/100V
C12 100PF/100V
C13 100PF/100V
C14 100PF/100V
C15 100PF/100V
C16 100PF/100V
C17 100PF/100V
C18 100PF/100V
CR8
CR9
CR10
CR11
XU1 20 PIN ZIF
C3 .01
FIRMWARE
U6 2732/ 2764 8000-9FEF
DATA GATE
U5 74LS244
C4,19 21 .01
C5 47/10V
CR3
CR4
C2 .1
R2 4.7K
R3, 470
R4, 470
DS1
DS2
SEL A 14
SEL B 13
INTERLOCK 70
88 A0
82 A1
76 A2
67 A3
64 A4
85 A5
79 A6
73 A7
66 A8
68 A9
61 A10
65 A11
58 A12
52 D01
49 D02
46 D03
43 D04
40 D05
37 D06
34 D07
31 D08
47 C3
1 +5V
2 +5V
3 +5V
28 +5V
22 GND
23 GND
26 GND
71 GND
72 GND
19 INTER-LOCK

-002 SHOWN

APPROVALS:	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	DATA I/O	
PROJ. ENG.	TOLERANCES DECIMALS .X ± .XX ± .XXX ± ANGULAR ± DO NOT SCALE DRAWING	TITLE SCHEMATIC DIAGRAM, PROGRAM TEST ADAPTER SERIES 20/24	
ENG. MGR.			
Q.C.	DRAWN BY A. K.	SIZE D	CODE IDENT NO 54193
DATE	CHECKED BY: S. Gentil 4/5/3	SCALE NONE	DRAWING NO 30-701-0046
			SHEET 2 OF 2